

CHAINSTATE-X: Transmedium Photonic Optimization Substrate

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Abstract

CHAINSTATE-X is a programmable heterogeneous physical substrate that maps CHAINSTATE energy landscapes onto optical, optoelectronic, phononic, thermodynamic, and—experimentally—QED-boundary degrees of freedom under a common RISC-V executive and a common CS.PHYSOPT instruction-set architecture. The paper defines a seven-layer architecture, an energy-landscape intermediate representation, a substrate-neutral runtime with classical CMOS fallback on every path, and a two-gate execution model that separates pre-execution authorization (EXEC_AUTH) from post-verification retirement. The device family spans a commercially manufacturable core—a RISC-V executive with a photonic tensor engine, a photonic Ising engine, a photonic reservoir, and a memristive persistent-state layer, targeting process kits at AIM Photonics, imec, LioniX, IHP, and Fraunhofer HHI—and a research-grade frontier comprising a diamond phononic-crystal substrate and three independent laboratory configurations for Casimir cavity, dynamic Casimir effect, and sonoluminescence experiments. Constitutional guarantees inherited from Paper XVII (V1 - V9 vetoes, SENTINEL five-gate pipeline, ALLOW gate, egress filter Γ) are enforced in hardware across every substrate, and every substrate has a specified falsification threshold. Performance figures use an E/A/T evidence taxonomy: E for experimentally demonstrated on CHAINSTATE-X hardware, A for literature anchor from a cited external experiment, T for CHAINSTATE-X target or specification not yet demonstrated.

Keywords

Programmable Photonic Circuits, MZI Mesh, Photonic Ising Machine, Hopfield-Inspired, Photonic Reservoir Computing, Phononic Bandgap,

*A Programmable Heterogeneous Physical Substrate That Maps CHAINSTATE Energy Landscapes onto Optical, Optoelectronic, Phononic, Thermodynamic and—Experimentally—QED Boundary Degrees of Freedom, with a RISC-V Executive, a Common CS.PHYSOPT Instruction Set, and Hardware-Enforced Constitutional Guarantees Inherited from Paper XVII.

Optomechanical Coupling, Casimir Cavity, Dynamic Casimir Effect, Sonoluminescence, RISC-V Executive, CS.PHYSOPT ISA, Energy-Landscape IR, Eigenmode-Selective computation, Polarisation State Space, WDM, Entropy Production, Memristive Persistent State, Lindblad Open-System Dynamics, Constitutional Silicon, Deontic Layer, Base 8453

1. Introduction

1.1. What Is Natural on Photons

Photons compute what electrons do awkwardly: parallel linear transformations at line-rate, spectral filtering, optical multiplication by amplitude and phase, and superposition of tens of channels through a single guide. The linear phase of transformer attention, of graph-Laplacian smoothing, of large associative retrieval, and of every second-order energy-landscape minimisation is the photonic sweet spot. CHAINSTATE-X organises these operations under one ISA and one energy-landscape IR.

1.2. What Paper XVII Established

Paper XVII (CHAINSTATE-1) shipped an RV64GC executive, 23 CS.* compute families, a hardware-enforced Deontic layer with V1 - V9 vetoes, SENTINEL five-gate pipeline, ALLOW gate, and Γ egress filter, and a Base 8453-anchored provenance chain. CHAINSTATE-X inherits all of these without modification and adds only the physical-substrate compute plane.

1.3. What CHAINSTATE-X Adds

One additional ISA family, CS.PHYSOPT; six additional physical substrates P1 - P6; one additional IR (energy-landscape IR); and a substrate-neutral runtime that dispatches CS.* operations to whichever substrate the compiler's cost model prefers, with classical CMOS fallback preserved on every path.

1.4. The Design Equation

$$\min E(x) + \lambda_t \cdot \tau + \lambda_e \cdot \varepsilon + \lambda_s \cdot \dot{S} + \lambda_r \cdot R$$

where τ is time to solution, ε is energy per operation, $\dot{S}$ is entropy production, R is a per-family risk metric. The λ multipliers are dispatched-instruction hints from the CS.PHYSOPT manifest.

1.5. What This Paper Delivers

A specification-level description of the seven-layer architecture, its programmable device family P1 - P6, the CS.PHYSOPT ISA that names every physical operation, and the constitutional gates that survive from Paper XVII. Performance figures are labelled with the v0.2 evidence taxonomy: E for experimentally demonstrated

on CHAINSTATE-X hardware, A for literature anchor from a cited external experiment, T for CHAINSTATE-X target or specification not yet demonstrated.

2. Architecture

2.1. The Seven Layers

L0 physical substrate hosting (packaging, laser sources, cooling); L1 - L4 parallel physical substrates (P1 photonic linear, P2 photonic Ising, P3 photonic reservoir, P4 phononic, and, separately, P5 thermodynamic + memristive persistent state); L4.5 CS.PHYSOPT ISA; L5 RISC-V control; L6 CHAINSTATE application layer. P6 is not a co-resident substrate but a family of three independent laboratory configurations (Section 10).

2.2. The Three Design Axes

Compute physics · thermodynamic budget · constitutional discipline. Every substrate is instrumented on all three axes, and every dispatched instruction carries an epistemic class, a tolerance vector, and a Deontic authorisation artefact.

2.3. Dispatch Model

Decision-tagged instructions complete the ALLOW gate before physical execution and must present an EXEC_AUTH decision from the verified Deontic path (see Section 14, Section 22). Only after physical execution, measurement and verification does the instruction reach the architectural retirement checkpoint.

2.4. Substrate-Neutral Runtime

Every CS.* operation has at least one CMOS realisation. The physical substrates are cost-model preferences, not required paths. A CS.PHYSOPT.NOTAVAIL exception falls back to CMOS for any operation whose physical target is disabled, out of trust region, or missing calibration.

3. The Energy-Landscape Intermediate Representation

3.1. The General Form

Every CS.* operation reduces to minimisation of an energy functional over a configuration space with substrate-visible coefficients (J, h, V), a tolerance vector, and a substrate hint:

$$\text{EL-IR} \langle \text{op} \rangle = \{J, h, V, \text{substrate_hint}, \text{tolerance}, \text{epistemic_class}\}$$

3.2. The Unified Open-System Model

Canonical state vector A · corrected 14 variables

The complete transmedium substrate is described by a unified Hamiltonian summing six substrate contributions:

$$H_{\text{total}} = H_{\text{ph}} + H_{\text{phn}} + H_{\text{EM}} + H_{\text{int}} + H_{\text{Cas}} + H_{\text{ctrl}} \quad (3). \text{ Because every physical substrate is an open system, } \rho \text{ evolves under the Lindblad master equation}$$

Continued

$d\rho/dt = -(i/\hbar)[H_{\text{total}}, \rho] + \sum_k \Gamma_k \cdot [L_k] \rho$ (4), with dissipator $[L] \rho = L \rho L^\dagger - \frac{1}{2}\{L^\dagger L, \rho\}$ (5).

The CS.PHYSOPT controller parameterises Hctrland the Lkoperators through the compile-time-known **14-variable state vector Λ** :

$$\Lambda = (\lambda, \varphi, p, m, t, T, B, E, \mu, \varepsilon, d, J, \kappa, \Omega)$$

wavelength λ , optical phase φ , polarisation p , spatial mode m , temporal mode t , temperature T , magnetic field B , electric field E , chemical potential μ , strain ε , cavity gap d , coupling J , loss rate κ , drive frequency Ω . Geometry is a derived configuration object, not one of the fourteen scalar state variables—a change from v0.1, which enumerated 12 elements while claiming the same 14-variable list.

3.3. Entropy Is a First-Class Hardware Telemetry Channel

Every substrate publishes $\dot{S}$, the local entropy production rate, on a per-instruction basis. The CS.PHYSOPT scheduler uses $\dot{S}$ as a live gate for trust-region behaviour and as a Deontic-layer feature for constitutional checks (Paper XVII Section 7).

3.4. The IR Is What the Compiler Emits

LLVM emits EL-IR from CS.* intrinsics. The runtime dispatches to a specific physical substrate driver, which sets Λ , mesh phases, coupling matrices, and pump powers as required. Substrate-neutrality is enforced by requiring every EL-IR emission to compile to CMOS as well as to the preferred physical substrate.

3.5. Worked EL-IR Mappings

The single most valuable v0.2 addition. Three worked examples walk a reader through input $\rightarrow$ EL-IR $\rightarrow$ physical state $\rightarrow$ measured output $\rightarrow$ verification for the three commercially defensible substrates.

3.5.1. Worked Example A · Attention/P1

Attention, P1 linear photonic mesh

EL-IR emission	Given Q, K, V , the compiler emits two linear EL-IR stages: score $S = QK_T / \sqrt{d_k} s$, followed by the value stage $Y = AV$ with $A = \text{softmax}(S)$. Each linear stage is dispatched to P1.
Encoding	Vector elements $\rightarrow$ optical amplitudes; matrix coefficients $\rightarrow$ calibrated mesh parameters (φ, κ) ; wavelength/polarisation/mode identify the multiplexed channels.
Physical execution	P1 implements each supported linear transformation as $E_{\text{out}} = U(\varphi, \kappa) E_{\text{in}}$. The electronic control path performs the intervening softmax between the two photonic stages (Section 5.5). Balanced photodetection produces the measured vector.

Continued

Measured output Verification	Photodetector samples $\hat{S}$ and $\hat{Y}$, digitised by the ADC. $\ \hat{Y} - Y_{\text{ref}}\ ^2 / \ Y_{\text{ref}}\ ^2 \leq \varepsilon_{\text{rel}}$, together with the declared absolute-error bound ε_{abs} . Reference Y_{ref} is computed in CMOS BF32 and released as part of the provenance receipt.
Exactness	The mathematical linear transformation is exact within the representational and calibration model; the implemented optical + electronic result is an approximate physical realisation subject to finite precision, loss, detector noise, and calibration error. The whole-attention mapping is not exact—softmax is inserted electronically. Cross-referenced from Section 5.6.

3.5.2. Worked Example B · MaxCut/P2

MaxCut, P2 photonic Ising OPO/OEO

EL-IR emission	For graph $G = (V, E, w)$, with $s_i \in \{-1, +1\}$ and cut value $C(s) = \frac{1}{2} \sum_{(i,j) \in E} w_{ij} (1 - s_i s_j)$, the compiler emits the Ising Hamiltonian $H(s) = -\sum_{(i,j) \in E} w_{ij} s_i s_j$, which is equivalent to maximising the cut up to an additive constant and sign convention. The mathematical reduction Max Cut $\rightarrow$ Ising is exact .
Encoding	$s_i \rightarrow$ OPO/OEO phase 0 or π ; $J_{ij} = w_{ij}$; $h_i = 0$ in the base problem; OEO feedback realises the coupling. Measured oscillator signs form the candidate cut.
Physical execution	OEO ring settles to a low-energy phase configuration; balanced photodetection reads phase parity per node.
Measured output	$\hat{s} \in \{-1, +1\}^n$ read out from photodetector signs after the OEO settling window.
Verification	Recompute the cut value classically from the measured spin vector and require $q = C(\hat{s})/C^* \geq 0.99$ (<i>i.e.</i> within 1% of the known/reference ground state on the reference random-graph benchmark).
Exactness	Reduction Max Cut $\rightarrow$ Ising: exact . Physical optimisation: approximate/probabilistic —finite-time OEO dynamics need not reach the global ground state. Success probability per single trial and restart discipline enter the end-to-end TTS (see Section 18.1). Cross-referenced from Section 6.1.

3.5.3. Worked Example C · Mackey-Glass/P3

Mackey-Glass prediction, P3 photonic reservoir

EL-IR emission	The reservoir is defined by $\dot{x} = f(x, u, \theta)$, $y = W_{\text{out}} x$, with only W_{out} trained (ridge regression). Mackey-Glass input samples $u(t)$ are injected into the optical reservoir; measured reservoir state $\hat{x}(t)$ is the physical feature representation.
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Continued

Encoding	$u(t) \rightarrow$ time-domain amplitude modulation into the SOA/SRR loop or OPO. Reservoir parameters θ (gain, feedback delay, pump power) are set at boot and remain fixed.
Physical execution	The physical reservoir evolves in real time at multi-GHz update rate; readout taps sample the state via photo detection at the configured cadence.
Measured output	$\hat{y}(t) = W_{\text{out}} \hat{x}(t)$.
Verification	Normalised root-mean-square error $\text{NRMSE} = \sqrt{\left\langle (\hat{y} - y_{\text{ref}})^2 \right\rangle} / \sigma(y_{\text{ref}}) < 0.1$. Stability: estimated largest Lyapunov exponent remains below the configured trust-region ceiling (Section 7.4).
Exactness Approximate	The physical reservoir is not claimed to reproduce the Mackey-Glass differential equation exactly; it is a hardware dynamical feature map trained to reproduce the target prediction. Cross-referenced from Section 7.1.

4. The Four Tiers of Commercial Defensibility

4.1. Tier Definitions

Tier T1 (P1, P2, memristive P5): commercially manufacturable today. Tier T2 (P3): research-grade, laboratory-first, path to commercial. Tier T3 (P4): laboratory hardware with published physics results but no shipping product analogue. Tier T4 (P6-A/P6-B/P6-C): three mutually independent QED-boundary laboratory configurations, none of them a shipping product; see Section 10.

4.2. Why the Tiers Are Ordered This Way

T1 revenue funds T2 development; T2 characterisation feeds T3 laboratory hardware; T4 remains scientific inquiry. Nothing in T2 - T4 is required to ship T1 devices.

4.3. Compile-Time Enablement

Every tier is enabled or disabled at compile time via the CS.PHYSOPT manifest. A T1-only build produces bit-identical software to a T3 build restricted to T1 substrates.

4.4. Additivity and Fail-Soft Semantics

Enabling a higher tier never disables a lower tier. A CS.PHYSOPT.NOTAVAIL exception on a higher-tier substrate falls back to the next lower tier without operator intervention.

5. P1 · Linear Photonic Accelerator

5.1. Physical Basis

128×128 MZI mesh on the AIM Photonics SiN or SOI PDK [1] [2]. Each mesh cell is a Mach-Zehnder interferometer with two phase shifters, calibrated to the reacha-

ble subgroup of $U(2)$. Cascaded 128×128 realises programmable unitary linear transformations. The mesh + electronic-nonlinear architecture concept follows the seminal deep-learning-with-coherent-nanophotonics demonstration [3] and its device-family successors (Lightelligence PACE, Lightmatter Enviser) [4] [5].

5.2. Mesh Topology

Clements rectangular architecture with post-fabrication remeshing to correct for imperfect beam splitters. Total mesh depth 128; per-cell insertion loss ≤ 0.09 dB target.

5.3. Microring Bank as WDM Matrix Multiplier

A parallel microring bank multiplies 16 WDM channels per waveguide against a stored key matrix, delivering the linear phase of CS.EMB and the associative-retrieval phase of CS.MEM at line rate.

5.4. Polarisation and Mode as Extra Dimensions

Aggregate channels vs transformation rank · separated

P1 exploits polarisation TE/TM and spatial-mode multiplexing to add channel opportunities per waveguide. Reconfigurable on-chip polarisation generation and analysis is now foundry-mature [6]; AIM Photonics' PDK supports TE and TM in its foundry ecosystem [1] [7]. Polarisation and spatial mode are exposed to the CS.PHYSOPT ISA as independent state variables (Section 12).

Channel-count vs transformation-rank separation. The device combines **2 polarisations $\times$ 2 spatial modes $\times$ 16 wavelengths $\times$ 128 waveguides = 8192 multiplexed channel opportunities** (corrected from v0.1's erroneous "4-polarisation-mode $\times$ 16-wavelength $\times$ 128-waveguide" phrasing). **8192 is an aggregate multiplexed channel-opportunity count, not the rank of the programmable linear transformation (see Table 1).**

The transformation dimension per independently configured wavelength/polarisation/mode block is **Nmesh = 128**. For a single 128×128 mesh block, $\text{rank}(W) \leq 128$. If the system uses independently controlled blocks, the aggregate 8192 figure represents simultaneously addressable multiplexed optical channel under the assumed mode-demultiplexing and crosstalk constraints; it does not imply an 8192-dimensional arbitrary dense linear transform. This same clarification appears in Section 5.7 and Section 12.3.

Table 1. v0.2 declared engineering assumptions. Values marked TBD are gated on measurement and not claimed as characterised. Crosstalk fields are explicitly not populated with invented numerical values.

Parameter	v0.2 declared assumption	Status
Waveguides	128	T
WDM channels	16	T
Polarisations	TE/TM	T
Spatial modes	2 (LP0,1 · LP1,1)	T
Aggregate multiplexed channels	8192	T
Dense transform dimension	128×128 per block	T
WDM spacing	200 GHz	A
Wavelength range	1530 - 1565 nm (C-band)	A

Continued

End-to-end mesh loss	≤12 dB target	T
Polarisation crosstalk	TBD experimentally	T
Spatial-mode crosstalk	TBD experimentally	T
WDM crosstalk	TBD experimentally	T
Parameter	v0.2 declared assumption	Status
Calibration method	per-MZI phase/amplitude + post-fab remesh [1]	T

5.5. Nonlinear Activations by Optoelectronic Conversion

P1's linear engine terminates in balanced photodetectors that convert optical amplitude to electronic signal. A nonlinear activation (ReLU, sigmoid, tanh, softmax) is inserted at the photodetector output in electronic form; the electronic result drives phase shifters for the next-layer MZI mesh via a Mach-Zehnder modulator. This is the standard photonic-linear + electronic-nonlinear architecture originating with Shen *et al.* (2017) [3] and now instantiated in shipping products (Envise, PACE), and reaches ~200 ps per-mesh latency.

5.6. CS.* Mapping

P1 executes the **linear phase** of CS.ATTN ($Q \cdot K^T$ and $\text{softmax}(\cdot) \cdot V$, where softmax happens electronically between the two photonic stages—see Section 3.5.1), CS.EMB (embedding table lookup as sparse matrix-vector), CS.MEM (associative retrieval as top-k against a stored key matrix), CS.MATH linear-algebra primitives, CS.SCI FFT/wavelet transforms, and the linear phase of CS.PERCEPT convolutional operators.

5.7. P1 Target Metrics

P1 target metrics · channel-count language corrected · E/A/T added. The 8192 figure is aggregate multiplexed channels (see Section 5.4); the 128×128 figure is the transformation dimension per block. Metric provenance is now labelled with the v0.2 evidence taxonomy.

Metric	Value	Basis	Status
Peak throughput	≥200 GOPS per block	128×128 mesh @ 1 GHz PD rate	T
Mesh latency	~200 ps	photonic linear stage	A
Insertion loss	≤12 dB end-to-end target	AIM Photonics SiN PDK [1]	T
MZI count	40,000+	128×128 Clements	T
Transformation dimension	128 (per block)	single mesh block rank ≤ 128	T
Aggregate channels	8192 multiplexed	$128 \cdot 16 \cdot 2 \cdot 2$	T
PD rate	1 GHz	balanced photo detection	A
Attention target	Paper XVII CS.ATTN peak conservative	128×128 mesh + 1 GHz PD	T

6. P2 · Photonic Ising Machine

6.1. Physical Mapping

Every quadratic unconstrained binary optimisation (QUBO) admits an exact Ising reduction. See Section 3.5.2 for the worked EL-IR mapping example $G \rightarrow \text{QUBO} \rightarrow \text{Ising} \rightarrow \text{OEO phases} \rightarrow \hat{s} \rightarrow C(\hat{s})$. The mathematical reduction MaxCut $\rightarrow$ Ising is **exact**; the physical optimisation is **approximate**, subject to finite-time OEO dynamics that need not reach the global ground state. Verification uses the classical recomputed cut value $C(\hat{s})/C^* \geq 0.99$.

6.2. The Optoelectronic Ising Architecture

Optoelectronic-oscillator (OEO) rings implement the Ising fabric. Each spin is an OEO whose steady-state phase is either 0 or π , corresponding to $s = +1$ or $s = -1$. Couplings J_{ij} are realised by programmable electro-optic modulators in the OEO feedback path. External biases h_i are additive modulations to the pump. The OEO settling time is ≈ 150 ns [8].

6.3. CS.* Mapping

P2 executes CS.GRAPH partitioning, CS.FOL clause-conflict analysis, CS.ENG constraint satisfaction, CS.FAB assignment problems, CS.ISO isomorphism candidate ranking, and CS.EML QUBO-shaped market-design auctions.

6.4. Scale and Connectivity

256 fully-connected spins in the base variant; 41 k sparse spins via embedded-graph techniques from D-Wave literature [9]–[11]. Neither number is claimed as an experimental CHAINSTATE-X result—see the E/A/T column below.

6.5. Eigenmode/Spectral-Gap Control

The CS.PHYSOPT.MODE.SELECT/SUPPRESS/COUPLE instructions expose the spectral gap to software as a compile-time-tunable cost function. Higher spectral gap $\rightarrow$ shorter settling time; lower spectral gap $\rightarrow$ less compute power but broader landscape exploration.

6.6. P2 Target Metrics · E/A/T Taxonomy

P2 metrics · evidence provenance separated per reviewer bonus recommendation

v0.1 mixed measurements taken on different physical systems in one table (256 spins from a 2025Hopfield-inspired result, 150 ns from an optical Ising result, 0.986 fidelity from a 32-spin demonstration, 65,536 embedded spins from a D-Wave precedent). v0.2 separates these into E (experimentally demonstrated on CHAINSTATE-X hardware), A (literature anchor from a cited external experiment), and T (CHAINSTATE-X target/specification not yet demonstrated).

Metric	Value	Basis	Status
P2 coupling fidelity	0.986	32-spin optical demo [8]	A

Continued

256-spin fidelity	≥ 0.986 target	CHAINSTATE-X extrapolation	T
Optical Ising evolution	≈ 150 ns	OPO settling time [8]	A
CHAINSTATE-X 256-spin evolution	≤ 500 ns acceptance criterion	engineering target	T
Fully-connected spins	256	P2 fabric target	T
Sparse (embedded) spins	41 k	D-Wave embedding literature [12]	A
Coupling power draw	~ 4 mW/nonlinear coupler	OEO datasheet-class target [9]	T
Time-to-solution	end-to-end value TBD (Section 18.1)	Requires load/pro- gram/read/verify	T

7. P3 · Photonic Reservoir**7.1. Physical Basis**

The physical reservoir realises a hardware dynamical system $\dot{x} = f(x, u, \theta)$ with a trainable linear readout $y = W_{\text{out}} x$. Silicon-photonic reservoir computing was demonstrated experimentally by Vandoorne *et al.* (2014) [13] on a chip that trained only W_{out} and reached ≥ 12.5 Gbit/s. See Section 3.5.3 for the Mackey-Glass EL-IR mapping. The reservoir is **not** claimed to reproduce a given target differential equation exactly; it is a nonlinear feature map trained to match the target prediction.

7.2. Photonic-Reservoir Implementations

Two candidate implementations extend the Vandoorne *et al.* (2014) silicon-photonic baseline [13]: an SOA/SRR delay-loop reservoir (SOA gain medium + fibre or on-chip delay + partial output coupling) and an OPO-based Kerr-nonlinear reservoir. Both give multi-GHz update rates. Only W_{out} is trained (ridge regression).

7.3. CS.* Mapping

P3 executes CS.TWIN evolution steps, CS.NEURO temporal classification, CS.FREE energy-based generation, CS.PERCEPT temporal filtering, CS.MARK annotation-quality scoring, and CS.META meta-learning adaptation.

7.4. Online Stability Estimator and Trust-Region Controller · REVISED**Explicit Lyapunov control algorithm**

v0.1 described the scheduler as one that *continuously monitors* λ_1 and refuses production traffic when it exceeds a fuse-locked ceiling. That is conceptually right but not an algorithm. v0.2 specifies the estimator, observation window, uncertainty margin, sampling cadence, decision rule, and fallback sequence in full.

Symbols. $\hat{\lambda}_1(t)$ estimated largest Lyapunov exponent · W_L sliding observation window · Δt_s sampling cadence · u_{λ} estimator uncertainty bound (one-sided) · λ_{fuse} immutable production ceiling (fuse-locked) · δ_{λ} safety margin.

Continued

Estimator. Nearest-neighbour divergence estimator:

$\hat{\lambda}_1 = d/d\tau \left[(1/M) \sum_{k=1}^M \ln(\delta x_k(\tau)/\delta x_k(0)) \right]$. Reservoir state samples are drawn every Δt_s from the P3 photodetector taps; nearest-neighbour pairs are maintained in a sliding buffer of length W_L .

Decision rule. $\hat{\lambda}_1 + u_{\lambda} < \lambda_{\text{fuse}} - \delta_{\lambda} \Rightarrow \text{ALLOW}$ production traffic. Otherwise, the scheduler enters the fallback sequence below.

Fallback sequence on violation. The scheduler (1) stops accepting new production reservoir traffic; (2) completes or invalidates the current measurement according to the instruction's execution class; (3) resets/reseeds the reservoir; (4) optionally reduces the configured gain/pump parameter within the manifest's characterised range; (5) reruns characterisation (drift-check); (6) otherwise raises CS.PHYSOPT.NOTAVAIL and falls back to CMOS.

Numerical values. W_L , Δt_s , u_{λ} , and the initial λ_{fuse} are **configuration parameters** established during P3characterisation, **not** measurements. The production image stores the resulting values alongside P3_lyapunov_ceiling in the CS.PHYSOPT manifest. Initial characterisation defaults are engineering starting values, not yet experimentally validated (status T).

7.5. P3 Target Metrics

Metric	Value	Basis	Status
Reservoir nodes	≥ 100	SOA/SRR loop target	T
Update rate	GHz-class	microring linewidth [14]	A
Trained parameters	only W_{out}	reservoir-computing standard	A
Nonlinearity	Kerr $\chi(3)$, saturable SOA	photonic implementations	A
Mackey-Glass NRMSE	< 0.1	falsification threshold (Section 22)	T
λ_1 trust ceiling	fuse-locked λ_{fuse}	operator-set at BIOS	T

8. P4 · Phononic Substrate

8.1. Physical Basis

Diamond phononic crystal with 50 - 70 GHz bandgap and $Q > 105$ target. The phononic-bandgap-shielded acoustic-resonator concept is anchored to MacCabe *et al.* (2020) [15], which reported a 5 GHz silicon cavity with $Q \approx 5 \times 10^{10}$ and 1.5 s phonon lifetime; CHAINSTATE-X Section 8 targets the 50 - 70 GHz diamond variant (status T; Section 21.1 R4 falsification threshold applies). Phononic modes are quantised mechanical excitations that couple to the photonic layer through optomechanical interfaces (radiation-pressure coupling and cavity-enhanced phonon-photon scattering).

8.2. Optomechanical Cross-Substrate Coupling

Optomechanical coupling connects P4 to P1/P3 through a shared cavity mode; phonon populations modulate the cavity optical frequency, and photonic drives populate specific phonon modes. This provides a thermodynamically slower channel

for states that must persist across reservoir resets.

8.3. CS.* Mapping

P4 exposes CS.PHYS (18 × phonon relaxation), CS.CFIELD (curved-space phonon transport), CS.CMTS (cross-medium transduction), and CS.SENTRY (vibration-based tamper detection).

8.4. P4 Target Metrics

Metric	Value	Basis	Status
Bandgap centre	50 - 70 GHz	diamond phononic literature [15]	A
Q factor	>105	cited phononic-bandgap cavity [15]	A
Feature size	20 nm	e-beam lithography	T
Optomechanical coupling	cavity-shared with P1/P3	reference optomechanical devices	A
Phonon-relaxation speedup	18×	characterisation target	T

9. P5 · Thermodynamic and Memristive Persistent State

9.1. Physical Basis

HfO2memristive crossbar delivers persistent physical state with 106 analog levels per cell and 10 yr retention. Entropy-production channel $\dot{S} \geq 0$ published per instruction; heat flux $J_q \cdot \nabla T/T_2$ feeds the CS.PHYSOPT scheduler’s thermodynamic cost model.

9.2. CS.* Mapping

P5 executes CS.PROV persistent-provenance state, CS.ID identity registers, and CS.HUMANlong-horizon interaction memory.

9.3. P5 Target Metrics

Metric	Value	Basis	Status
Analog levels per cell	106	STOC memristor characterisation	A
Write energy	nJ/write	cited HfO2crossbar	A
Retention	10 yr	cited HfO2crossbar	A
Endurance target	1010 cycles	engineering target	T

10. P6 · Three Independent QED-Boundary Laboratory Configurations · REVISED

P6 restructured as P6-A/P6-B/P6-C · mutually independent labs

v0.1 presented Casimir, DCE, and sonoluminescence as three sub-layers of a single P6 tier, and Section 15.3 described the CHAINSTATE-P3 device as shipping all three together. That framing invited the reviewer to ask about the physical interface between P6 and the room-temperature photonic system, and left ambiguous whether the three configurations were meant to coexist.

Continued

v0.2 restates the three as **P6-A · Casimir MEMS cavity**, **P6-B · superconducting DCE laboratory**, and **P6-C · sonoluminescence reservoir**. Each is a **mutually independent experimental configuration**. None of the three is assumed to coexist with the others in a production system, and none is claimed as a compute-power source.

Section 15 device-family language updated in parallel: P3 is now described as *the first research-grade host capable of interfacing to external P4/P6 laboratory modules*, not as a device that ships P4 + P6 together.

10.1. P6-A · Casimir MEMS Cavity

Purpose. Tunable boundary condition, cavity-mode selection, nanomechanical sensing, ultra-small force sensing.

Configuration. Room-temperature photonic PIC → optical probe/coupler → tunable Casimir cavity with MEMS gap actuator → optical readout at the photonic layer. A parallel capacitive MEMS readout feeds the control-side ADC. The Casimir force between ideal parallel plates is $F/A = -\pi 2\hbar c / (240d_4)$; Lifshitz theory handles the realistic material case [16]-[18].

Interface to the room-temperature photonic system. The MEMS cavity attaches to a dedicated experimental port on the photonic PIC. Optical probe light couples in, cavity-modulated light couples out, and the MEMS gap actuator is driven by the control-side ADC/DAC pair. Nothing in P6-A enters the P1/P2/P3 compute fabric as decision-tagged evidence.

Status. Physically removable module. Not on the CHAINSTATE-P1 or CHAINSTATE-P2 commercial base variants. Never accepted as evidence for any decision-tagged retirement.

10.2. P6-B · Superconducting DCE Laboratory

Purpose. Dynamic Casimir effect (DCE) research—generation of photons from vacuum by rapid boundary-condition modulation. Anchored to the 2011 Nature demonstration [19].

Configuration. A **cryogenic laboratory configuration**, not a room-temperature photonic compute substrate. The DCE process is hosted on a superconducting circuit with RF boundary modulation and observed as two-mode squeezed radiation.

Interface to the room-temperature photonic system. Room-temperature control electronics → RF/microwave drive chain → cryogenic superconducting circuit → microwave/photonic measurement chain → room-temperature ADC/data-acquisition interface. **DCE-generated photons never enter the P1/P2/P3 compute fabric** and are never accepted as decision-tagged evidence: the CS.PHYSOPT scheduler enforces this by an epistemic-class check at dispatch.

$$a_{\text{out}} = a_k \cdot a_{\text{in}} + \beta_k \cdot (a_{\text{in}})^\dagger \quad \text{with } n_k = |\beta_k|^2$$

Status. Laboratory configuration only. Never on the P1 or P2 commercial base variants. Never on a shared compute die.

10.3. P6-C · Sonoluminescence Reservoir

Purpose. Investigation of the collapsing bubble as a novel physical reservoir; anchored to the single-bubble sonoluminescence literature [20]. Bubble dynamics are exquisitely nonlinear, so the programme asks whether the collapsing bubble’s optical spectrum constitutes a useful nonlinear reservoir that differs from the SOA-loop reservoir of Section 7.

Configuration. Benchtop laboratory module: liquid cell (degassed water or D₂O) + piezoelectric ultrasonic transducer + single-bubble stabilization optics + high-speed spectrometer/photodetector.

Interface to the room-temperature photonic system. Liquid cell + piezo ultrasonic transducer + bubble-stabilisation optics + spectrometer/photodetector → optical fibre/PIC interface → room-temperature measurement/control system. The PIC does **not** host the liquid cell; the coupling is through a dedicated fibre feed.

Status. Research programme with a clear falsification criterion—either the reservoir’s output scores correlate with useful CS.* classifications or they do not (Section 22.4). Never on the P1 or P2 commercial base variants.

10.4. P6 Discipline · Mutually Independent, Never Coexisting

P6-A, P6-B, and P6-C are **mutually independent experimental configurations**. None of the three is required to be present for the others to function. They are **not assumed to coexist in a production system**. The variant matrix (Section 15.6) reflects this explicitly. The phrase “P6 substrate” is retired; only the three sub-configurations are referenced in v0.2.

11. Eigenmode-Selective Computation as First-Class ISA

11.1. The Mathematical Framing

Every physical substrate has structured eigenmodes: optical cavity resonances, phononic-crystal band gap edges, OEO limit-cycle phase attractors. CHAINSTATE-X exposes these eigenmodes as first-class ISA objects—instructions that select, suppress, or couple specific eigenmodes execute in a compact number of cycles rather than requiring full-mesh reprogramming.

11.2. Eigenbasis Geometry

The compiler chooses a substrate-appropriate eigenbasis at EL-IR emission time. Photonic eigenmodes are labelled by (λ, m) ; phononic eigenmodes by (Ω, k) ; OEO eigenmodes by phase attractor $s \in \{0, \pi\}$.

11.3. Cross-Substrate Eigenmode Transport

The CS.PHYSOPT.MODE.COUPLE instruction moves state between eigenbases on adjacent substrates (photonic → phononic, phononic → OEO). Transport fidelity is bounded by the interface’s transduction budget and is published as part of the substrate manifest.

12. The Photonic State Vector and ISA Exposure

12.1. The State Vector

The 14 scalar state variables of Section 3.2 map to ISA-visible operands.

$\Lambda = (\lambda, \varphi, p, m, t, T, B, E, \mu, \varepsilon, d, J, \kappa, \Omega)$. Every CS.PHYSOPT instruction accepts a subset of Λ as its operand vector, allowing the compiler to program the substrate at the physical-parameter level.

12.2. Polarisation as Computational Channel

TE and TM polarisation states multiply the channel count per waveguide by 2. Polarisation is exposed to software as the state variable p .

12.3. Wavelength-Division Multiplexing

Channel-count vs transformation-rank separation · third occurrence

16 WDM channels on the C-band grid (1530 - 1565 nm at 200 GHz spacing) carry 16 independent scalar elements per waveguide. Combined with 2 polarisations (TE/TM), each waveguide carries 32 independent scalars simultaneously. The 128×128 mesh's aggregate multiplexed channel count becomes $128 \times 32 = 4096$; adding **2 independent spatial modes (LP0,1 and LP1,1)** gives **2 polarisations $\times$ 2 spatial modes $\times$ 16 wavelengths $\times$ 128 waveguides = 8192 aggregate multiplexed channel opportunities. 8192 is the aggregate multiplexed channel-opportunity count, not the rank of the programmable linear transformation.** The dense-transform dimension is $N_{\text{mesh}} = 128$ per independently configured wavelength/polarisation/mode block. For a single 128×128 mesh block, $\text{rank}(W) \leq 128$. Same clarification appears in Section 5.4 and Section 5.7.

12.4. Temporal-Mode Encoding

Time-bin encoding assigns each pulse to a temporal slot, giving temporal-mode multiplexing orthogonal to wavelength, polarisation, and spatial mode. The 1 GHz photodetector rate of P1 sets the smallest usable temporal slot; P3 reservoir dynamics fill the temporal-mode dimension with reservoir state.

12.5. The ISA Exposure

The CS.PHYSOPT.STATE.LAMBDA/PHI/P/M/T instructions expose each of the 14 state-vector components to software. The compiler assigns compile-time values that the runtime propagates to the substrate driver.

13. The CS.PHYSOPT Instruction Set Architecture

13.1. Encoding

CS.PHYSOPT uses the RISC-V custom-1 opcode (0101011) with the sub-op field selecting family and operation. See Paper XVII Section 5 for the base CS.* encoding envelope.

13.2. The Ten Families

PHYSOPT.LINEAR (P1) · PHYSOPT.ISING (P2) · PHYSOPT.RESERVOIR

(P3) · PHYSOPT.PHONON (P4) · PHYSOPT.MEMRIST (P5) · PHYSOPT.CAVITY (P6-A) · PHYSOPT.DCE (P6-B) · PHYSOPT.SONOLUM (P6-C) · PHYSOPT.MODE (cross-substrate eigenmode transport) · PHYSOPT.STATE (14-variable state-vectoraccess).

13.3. Semantic Conventions

Every instruction carries an epistemic class $\in \{\text{DECISION, MEASUREMENT, RESEARCH, DIAGNOSTIC}\}$. Only DECISION-class instructions reach the ALLOW gate and produce a signed retirement receipt. RESEARCH-class instructions execute in a physically isolated resource envelope and their results are excluded from downstream decision-tagged operations by construction.

13.4. Full Instruction Reference (Excerpt)

Selected instructions—the complete reference is archived to the public Base 8453 anchor.

Mnemonic	Operands	Meaning
PHYSOPT.LINEAR.APPLY	rs1, rs2, rd	apply mesh $U(\varphi, \kappa)$ to E_{in}
PHYSOPT.ISING.SETJ	rs1, rs2	load coupling matrix J_{ij}
PHYSOPT.ISING.SETTLE	rd	OPO settle $\rightarrow$ measure $\hat{s}$
PHYSOPT.RESERVOIR.INJECT	rs1	amplitude-modulate $u(t)$ into reservoir
PHYSOPT.RESERVOIR.READOUT	rd	read reservoir state $\hat{x}$
PHYSOPT.PHONON.COUPLE	rs1, rs2	couple optomechanical mode
PHYSOPT.MEMRIST.WRITE	rs1, rs2	write analog value to crossbar
PHYSOPT.CAVITY.DCE_MODULATE	rs1, tag	P6-B research modulation
PHYSOPT.CAVITY.SONOLUM	rs1, tag	P6-C sub-variant only
PHYSOPT.MODE.SELECT	λi , tag	eigenmode select
PHYSOPT.MODE.SUPPRESS	λi , tag	eigenmode suppress
PHYSOPT.MODE.COUPLE	λi , λj	couple eigenmodes
PHYSOPT.MODE.QUERY	λi , rd	amplitude $\rightarrow$ rd
PHYSOPT.STATE.LAMBDA	rs1	set λ (wavelength)

14. RISC-V Interface and Compiler Pipeline · Two Execution Gates · REVISED

The RISC-V executive of CHAINSTATE-X is the Paper XVII Section 3 executive plus a CS.PHYSOPT decoder plus a physical-substrate scheduler. Software above the executive sees CS.PHYSOPT as a normal CS.* extension: LLVM emits CS.PHYSOPT instructions from a set of intrinsics, the runtime dispatches them,

and the fabric returns results through the retirement checkpoint of Gate B below.

Two-gate execution model resolves the Section 14 ↔ Section 22.1 contradiction

v0.1 Section 14 stage 4 called itself “retirement checkpoint” while Section 22.1 asserted that formal-verification properties require every instruction to reach retirement *before* any physical execution begins. The two statements are incompatible under a single meaning of “retirement”. v0.2 defines two distinct gates and reserves’ retirement’ exclusively for the post-verification gate.

Gate A · Pre-execution authorization checkpoint. Before physical execution: Decode → EL-IR → Manifest → Deontic authorization → **EXEC_AUTH** → physical execution. Gate A checks substrate target, epistemic class, tolerance, safety constraints, and resource availability. Every instruction **MUST** pass Gate A before the fabric may begin physical execution.

Gate B · Post-execution retirement checkpoint. After: physical execution → measurement → verification → **RETIRE**. Only at Gate B is the architectural state updated and the provenance receipt HMAC-signed and anchored to Base 8453.

Section 22.1 SVA properties (see Section 22) are rewritten around EXEC_AUTH and RETIRE as distinct checkpoints.

14.1. The Compiler Pipeline · Seven Stages · v0.2

Stage numbering unchanged from v0.1; stage 4 is renamed and its scope restricted to **pre-execution authorization**. “Retirement” now refers exclusively to stage 7.

Stage	Name	Content
1	Source	CS.* runtime call · e.g. $cs_attn(Q, K, V)$ or $cs_graph_partition(G)$
2	LLVM intrinsic	e.g. $@llvm.cs.attn(Q, K, V, tolerance)$
3	EL-IR emission (Section 3.4)	$(J, h, V) +$ substrate hint + tolerance vector
4	Pre-execution authorization checkpoint (Gate A)	CS.PHYSOPT scheduler consults manifest; chooses substrate; verifies Deontic; costs per equation (9); emits EXEC_AUTH decision before any physical execution begins
5	Substrate driver	set $\Lambda = (\lambda, \varphi, p, m, t, T, B, E, \mu, \varepsilon, d, J, \kappa, \Omega)$
6	Physical execution	light propagates through mesh; OEO settles; reservoir evolves; phonon transfers; memristor writes
7	Measure + verify + retirement checkpoint (GateB)	photodetect; ADC; RISC-V verifier; provenance HMAC receipt; Base8453 anchor; RETIRE —architectural state update

14.2. The Manifest

The runtime physical-substrate manifest is populated at BIOS from a fuse-locked device-inventory ROM and carries per-substrate calibration, trust-region parameters (Section 7.4), authorised epistemic-class list, and substrate availability. The manifest is one of Gate A’s inputs.

14.3. Software-Visible Interface

Software sees a normal CS.* dispatch envelope. The two-gate structure is invisible to application code except through the provenance receipt returned at RETIRE, which carries the EXEC_AUTH decision hash from Gate A.

14.4. Provenance Receipts Include Substrate ID and Both Gate Hashes

Every retirement receipt now carries: substrate ID; EXEC_AUTH decision hash from Gate A; measurement result; verification result; HMAC over the combined structure; Base 8453 anchor txhash. This is the substrate's canonical audit artefact.

15. Device Family · REVISED Variant Language

P3/P6 device-family language corrected

v0.1 Section 15.3 described CHAINSTATE-P3 as the *first variant to ship P4 phononic + P6 QED experimental modules*. Taken with the Section 10 P6 revisions (P6-A/P6-B/P6-C as three mutually independent laboratory configurations), that phrasing became inconsistent.

v0.2 uses this language throughout Section 15: **P3 is the first research-grade host capable of interfacing to external P4/P6 laboratory modules. P6-A, P6-B, and P6-C are mutually independent experimental configurations and are not assumed to coexist in a production system.** The variant matrix reflects this: no shipped device asserts all three P6 configurations simultaneously.

15.1. CHAINSTATE-P1 · Commercial Linear-Photonic Accelerator

Positioning. Entry-level commercial device. First shipping variant. Direct commercial competitor to Lightelligence PACE2, Lightmatter Enviser, Saliency Labs' TDM engine—all built on the MZI-mesh + electronic-nonlinear architecture of [3]-[5]. **Physical.** P0 (co-packaged optics) + P1 (128 × 128 MZI mesh, WDM, TE/TM polarisation) + Paper XVII CHAINSTATE-1 fabric die as companion. P2 - P6 all disabled. **Package.** Full-height double-width PCIe 5 card, 200 W TDP, external laser input, 128 optical I/O fibres. **ASP.** USD 6000 - 9000. **Shipping.** Q3 2028: first commercial samples. **Foundry.** AIM Photonics SiN low-loss + TSMC N4/N3E for CS.* die.

15.2. CHAINSTATE-P2 · Optimisation-Focused SoC

Positioning. Adds Ising/reservoir substrates on top of P1. Targets combinatorial-optimisation buyers. Competes with D-Wave Advantage2, Fujitsu Digital Annealer, Toshiba SBM, Light Solver. **Physical.** P0 + P1 + P2 (256 fully-connected/41 k sparse Ising) + P3 (100-node OPO reservoir) + P5 (memristor persistence) + CS.* fabric die. P4 and all P6-A/B/C disabled. **Package.** Full-height double-width PCIe 5 card, 300 W TDP. **ASP.** USD 15,000 - 22,000. **Shipping.** Q1 2029. **Foundry.** AIM Photonics + imec III-V heterogeneous + TSMC N3E.

15.3. CHAINSTATE-P3 · Research-Grade Transmedium Host · REVISED Language

P3 as host, not integrated QED device

Positioning. Research + government + defence + sovereign-compute buyer. **The first research-grade host capable of interfacing to external P4 phononic and P6 laboratory modules.** P3 does not ship all P6 configurations simultaneously; the customer selects at most one of P6-A/P6-B/P6-C, and each of the three configurations arrives as a separately attached module.

Physical. P0 + P1 + P2 + P3 + P4 (diamond phononic crystal with 50 - 70 GHz bandgap) + P5 + **one** of {P6-A Casimir cavity, P6-B DCE research port, P6-C sonoluminescence module}—customer-selected. CS.* fabric die included.

Package. 4U rack unit; requires 2 kW cooling; separately-cooled phononic + Casimir sections. P6-Bcryogenic laboratory configuration requires an external dilution-refrigerator envelope not included in the rack.

ASP. USD 180,000 - 350,000 depending on P6-A/B/C selection. **Shipping.** Q3 2029 first samples. **Foundry.** AIM Photonics + imec + custom diamond MEMS + Fraunhofer HHI photonic packaging.

15.4. CHAINSTATE-P4 · Phononic + P6-C Sonoluminescence Research Module

Positioning. Physics-research add-on to CHAINSTATE-P3. Not a stand-alone product. Combines the P4 phononic laboratory programme with the P6-C sonoluminescence configuration when the customer selects that P6 variant. **Physical.** Dedicated liquid-cell cavity with piezoelectric ultrasonic transducer array, degassed water or D2O working fluid, single-bubble stabilisation optics, high-speed spectrometer, PIC coupling. **Package.** Benchtop module with optical fibre coupling to CHAINSTATE-P3. **ASP.** USD 45,000 - 80,000 for the module (in addition to the P3 host). **Shipping.** 2030 in prototype form only. **Foundry.** Custom laboratory assembly; not fabless.

15.5. CHAINSTATE-X SoC · Full Integration Flagship

Positioning. The fully-integrated flagship. Every commercially manufacturable physical substrate P1-P5 on a single reference board with a 2.5D-packaged CS.* fabric die. **Optional** external attach of exactly one of P6-A, P6-B, or P6-C. **Physical.** P0-P5 all present; P6 optional external attach (one of A/B/C only); CHAINSTATE-1 CS.* fabric die (Paper XVII, 550 - 700 mm² TSMC N3E) bonded as a 2.5 D companion on a shared silicon interposer; HBM3E stacks × 2 for 48 GB working memory; CoWoS-L packaging. **Package.** Full-height double-width PCIe 5 card, 350 - 400 W TDP, active liquid cooling. **ASP.** USD 45,000 - 60,000 base configuration; USD 220,000 - 480,000 with any one P6 external attach. **Shipping.** Q2 2030. **Foundry.** TSMC N3E + AIM Photonics + imec + Lionix + IHP mixed.

15.6. Variant Matrix · REVISED · P6 Column Is A/B/C Selection

Column P6 now represents which single P6-A/B/C configuration is shipped, not a simultaneous ownership of all three—indicates no P6 configuration; A, B, C in-

dicate exactly one selected.

Variant	P1	P2	P3	P4	P5	P6 selection	CS.* die	First silicon
CHAINSTATE-P1	✓	—	—	—	partial	—	✓	Q3 2028
CHAINSTATE-P2	✓	✓	✓	—	✓	—	✓	Q1 2029
CHAINSTATE-P3	✓	✓	✓	✓	✓	one of A/B/C	✓	Q3 2029
CHAINSTATE-P4module	—	—	—	—	—	C only	—	2030
CHAINSTATE-X SoC	✓	✓	✓	✓	✓	opt. one of A/B/C	2.5 D CoWoS	2030

16. Materials Stack and Fabrication Options

16.1. Materials-by-Layer Table

Materials chosen for manufacturability at established foundries or in established laboratory processes with published performance envelopes [2].

Layer	Material	Process	Basis
P1 mesh	SiN or SOI	AIM Photonics PDK 5.5	commercial
P1 laser source	III-V InP	imec heterogeneous	commercial
P2 OEO	SOI + III-V bonded	imec + AIM	commercial
P3 SOA loop	In Ga As P	III-V bonded	commercial
P4 phononic crystal	diamond, 20 nm features	e-beam lithography	laboratory
P5 memristor	HfO ₂	back-end integration	cited
P6-A Casimir cavity	silicon MEMS	custom fab	laboratory
P6-B DCE circuit	superconducting Al or Nb	custom cryogenic	laboratory
P6-C sonoluminescence	quartz cell + piezo	benchtop assembly	laboratory
CS.* companion die	TSMC N3E	Paper XVII	commercial

16.2. Foundry Options

Primary foundries: AIM Photonics (P1 mesh, packaging), imec (III-V bonding), Lioni X (SiN low-loss), IHP (BiCMOS driver ICs), Fraunhofer HHI (packaging), TSMC N3E (CS.* die). Secondary sources documented per Section 17.1.

16.3. Fabrication Flow · Base P1 Variant

Nine-step flow: SiN waveguide layer → mesh definition → phase-shifter loading → microring bank → III - V bonding → detector integration → electrical top metal → laser attach → optical packaging.

17. Supply Chain

17.1. Critical-Path Components with Dual-Sourcing

AIM Photonics SiN + LioniX SiN as parallel PDKs; imec III - V + Fraunhofer HHI III-V as parallel bonding paths; TSMC N3E + Samsung SF3 as parallel N3-class options for the CS.* companion die. Diamondphononic-crystal fabrication triple-sourced across three e-beam-capable laboratories.

17.2. IP Licensing Per-Unit Cost

SiFive P670 or Andes AX65 RV64GC core IP: USD 3 - 6/unit at scale. AIM Photonics PDK royalty: USD 12 - 25/unit. Tenstorrent Tensix (used as CS.* companion accelerator on select variants): open-sourceISA, no per-unit licence.

17.3. First-Silicon Budget · CHAINSTATE-X SoC Full Variant

Line item	USD	Notes
Mask set (N3E, CS.* die)	\$34 M	TSMC N3E
MPW tape-out (P1 photonic)	\$0.9 M	AIM Photonics
MPW tape-out (P2/P3 III-V)	\$1.4 M	imec
Prototype packaging (CoWoS-L)	\$3.2 M	TSMC OSAT
Diamond phononic crystal lot	\$1.1 M	custom lab run
Casimir MEMS lot	\$0.6 M	silicon MEMS
Superconducting DCE circuit build	\$0.9 M	cryogenic lab build
Sonoluminescence cell prototypes	\$0.15 M	benchtop
Test & characterisation (12 months)	\$4.8 M	internal team
Total first-silicon budget	\$47.05 M	excludes NRE

18. Benchmark Protocol and Performance Figures · Formal TTS · REVISED

18.1. End-to-End Time-to-Solution · NEW Definition

Formal TTS definition

v0.1 presented a Max Cut figure of 150 ns and a $\sim 4000\times$ perf-per-watt ratio against D-Wave in the same table. The 150 ns is the OEO physical evolution/settling time; competitors are typically benchmarked on end-to-end time-to-solution, which includes loading, programming, readout, verification, and restarts. Comparing a physical evolution time against end-to-end solve times is not a like-for-like comparison. v0.2 defines TTS formally and separates the two rows in every relevant table.

Definition of one trial. $T_{\text{trial}} = T_{\text{load}} + T_{\text{program}} + T_{\text{evolve}} + T_{\text{read}} + T_{\text{verify}} + T_{\text{restart}}$

Definition of TTS. If $p_s(q)$ is the probability that one independent trial returns a solution satisfying quality threshold q , then the time to obtain success probability p^* is

$\text{TTS}(p^*, q) = T_{\text{trial}} \cdot \left[\ln(1 - p^*) / \ln(1 - p_s(q)) \right]$. **Quality threshold.** For MaxCut:

$q = C(\hat{s})/C^*$, with $q \geq 0.99$ corresponding to the paper's existing "within 1% of the reference ground state" wording. Same q used in the Section 22.4 falsification threshold.

Continued

Renamed rows in the benchmark table. The 150 ns entry is renamed **Physical evolution time**. A new row **End-to-end TTS @ 99% success, $\geq 99\%$ quality** is added; its value is currently marked TBD until the load/program/readout/verification times and single-trial success probability are experimentally established.

Withdrawn claim. The v0.1 Section 18.2 $\sim 4000\times$ vs D-Wave perf-per-watt ratio is withdrawn from v0.2 because it was derived from the physical evolution time rather than end-to-end TTS. Replacement text: *not yet established; physical-evolution target = 150 ns; end-to-end TTS TBD.*

18.2. Benchmark Table · E/A/T Status Column Added

Rows previously merging demonstrated components with target metrics are now separated. Numerical values from cited external experiments are labelled A; CHAINSTATE-X targets are labelled T; nothing on CHAINSTATE-X hardware has yet been experimentally demonstrated (no E rows).

Device	Class	MaxCut 256 T evolve	MaxCut 256 end-to-end TTS	Power/card	Constitutional Status	
Nvidia B200	General GPU	100 μ s (MCMC)	100 μ s+	1000 W	none	A
AMD MI450	General GPU	90 μ s	90 μ s+	1000 W	none	A
Google TPU v5p	Purpose GPU	300 μ s	300 μ s+	280 W	none	A
Groq LPU	Data flow SRAM	100 μ s	100 μ s+	400 W	none	A
Cerebras WSE-3	Wafer-scale	50 μ s	50 μ s+	15 kW	none	A
D-Wave Advantage 2	Quantum annealer	10 μ s (7 k qubits)	end-to-end TBD	25 kW	none	A
Fujitsu Digital Annealer 4	Digital annealer	50 μ s	50 μ s+	700 W	none	A
Toshiba SBM	Sim. bifurcation	40 μ s	40 μ s+	400 W	none	A
CHAINSTATE-P2	Constitutional	150 ns (physical evolution)	TBD experimentally	300 W	hw	T
CHAINSTATE-XSoC	Full transmedium	150 ns (physical evolution)	TBD experimentally	380 W	hw	T

T_{evolve} for CHAINSTATE-P2/CHAINSTATE-X SoC is the photonic OEO settling time [9] [12]. End-to-end TTS additionally counts T_{load} , T_{program} , T_{read} , T_{verify} , T_{restart} , and single-trial success probability against the $q = 0.99$ quality threshold; these are TBD experimentally.

18.3. Perf-per-Watt · $\sim 4000\times$ Claim Withdrawn

Perf-per-watt table restated. The v0.1 Section 18.2 perf-per-watt table gave a $\sim 4000\times$ ratio for MaxCut 256 against D-Wave, using the physical-evolution time as CHAINSTATE-X's figure of merit. v0.2 withdraws this ratio.

Workload	Best merchant device	CHAINSTATE-X SoC status	Status
MaxCut 256 (end-to-end TTS)	D-Wave Advantage2	not yet established · physical-evolution target = 150 ns	T
Twin-step BF16	Cerebras WSE-3	target $\geq 2.6 \times 10^6$ steps/s/W	T

Continued

128 × 128 dense matmul(photonic)	Lightelligence PACE2 [3]	comparable target (≈109 ops/s/W)	T
Constitutional receipt-signedops	—	only device with all ops signed	T

19. Game Theory of the Market and Classified Programmes**19.1. The Four Games**

G1 commercial photonic accelerator market · G2 combinatorial-optimisation market · G3sovereign-compute market · G4 classified programmes. CHAINSTATE-X strategically enters G1 first with P1, expands into G2 with P2, and offers G3/G4 buyers the P3 research host with selectable P6-A/B/C configuration.

19.2. The Classified-Programme Landscape (G4)

DARPA HIVE/DPRIVE/MOSAICS, UK ARIA, Euro HPC JU, and equivalent sovereign programmes are prospective buyers of the P3 research variant. The constitutional layer is the primary technical differentiator against merchant photonic accelerators.

19.3. Strategic Dimensions and Dominance Analysis

Six strategic dimensions: manufacturability, constitutional discipline, compute-density-per-watt, tolerance to non-Deontic customers, supply-chain-diversification, and ISA sovereignty. CHAINSTATE-X occupies dominance regions on constitutional discipline, ISA sovereignty, and supply-chain diversification; competes on manufacturability and compute-density-per-watt; and does not compete on tolerance to non-Deontic customers by design.

19.4. What CHAINSTATE-X Wins

Sovereign-compute contracts where hardware-enforced constitutional guarantees are required (Deontic V1 - V9 vetoes, SENTINEL 5-gate, ALLOW, I). CHAINSTATE-X is the only device family in this comparison with a hardware-enforced constitutional layer (Paper XVII Section 7).

19.5. What CHAINSTATE-X Does Not Win

Non-constitutional dense-inference workloads at scale, where B200/MI450/TPU v5p dominate on raw perf-per-watt. CHAINSTATE-X's response in G1 is to concede these workloads and target CHAINSTATE-native workloads instead.

19.6. The Classified-Programme Response Function

Sovereign programmes value: (a) auditable provenance chain; (b) hardware-enforced constitutional discipline; (c) supply-chain independence from any single foreign foundry. CHAINSTATE-X delivers all three by design.

20. Phase Timeline

Milestones

Milestone	Date	Status
Paper XIX v0.2 revision publication	14 Sep 2026	T
CS.PHYSOPT ISA specification frozen	Q1 2027	T
P1 MPW tape-out at AIM Photonics	Q3 2027	T
P1 first-silicon characterisation	Q1 2028	T
CHAINSTATE-P1 first commercial samples	Q3 2028	T
P2 MPW tape-out with III-V bonding	Q4 2028	T
CHAINSTATE-P2 first commercial samples	Q1 2029	T
P3 host qualification	Q2 2029	T
CHAINSTATE-P3 first research samples	Q3 2029	T
CHAINSTATE-X SoC full integration	Q2 2030	T
P6-A/B/C laboratory characterisation reports	2028-2031	T

21. Risk Register and Aggregate Exposure

21.1. Technology Risks

R1: MZI mesh loss exceeds 12 dB (P1). R2: OEO fidelity below 0.90 at 256 spins (P2). R3: reservoir Lyapunov exponent instability (P3). R4: diamond phononic crystal Q insufficient (P4). R5: memristor endurance below 108cycles (P5). R6: any P6-A/P6-B/P6-C laboratory result fails to reproduce the cited literature anchor. Each falsification threshold is spelled out in Section 22.4.

21.2. Fabrication and Supply Risks

Triple-source diamond phononic-crystal e-beam capacity; dual-source SiN PDK; dual-source III - V heterogeneous bonding; dual-source N3-class CS.* die manufacturing. Amkor SLIM and TSMCCo WoS-L as parallel advanced-packaging paths.

21.3. Regulatory and Market Risks

US export-control classification of the CS.PHYSOPT ISA and CHAINSTATE-X SoC. EU AI Act general-purpose model rules on downstream CHAINSTATE AGI applications. UK ARIA/Euro HPC procurement rules for the P3 research variant.

21.4. Constitutional Risks

Any post-silicon change to the Deontic policy ROM would require a public disclosure and a new anchor on Base 8453. The v0.2 policy ROM contents are public per Paper XVII Section 7.4.

21.5. Aggregate Risk Exposure

Aggregate technology-risk-adjusted first-silicon budget: 2.05 - 2.51 for merchant

competitors (Section 19.3). CHAINSTATE-X's constitutional-layer premium prices in against this exposure.

22. Formal Verification and Peer-Review Protocol

22.1. Formal-Verification Methodology · Two-Gate SVA · REVISED

Safety properties rewritten around EXEC_AUTH/RETIRE distinction

v0.1 Section 22.1 required every dispatched instruction to *reach the retirement checkpoint before any physical execution begins*, which was incompatible with Section 14's stage-4 → stage-6 → stage-7 ordering. v0.2 Section 14 defines two distinct gates (Section 14 REVISED) and Section 22.1 SVA properties are rewritten to match.

Every Deontic-layer block is formally verified with Cadence Jasper Gold + Synopsys VC Formal. Each V1-V9veto is expressed as an SVA assertion pair (liveness + safety) per Paper XVII Section 7.4. The CS.PHYSOPT decoder adds ten SVA assertion pairs—one per CS.PHYSOPT family (Section 13.2)—verifying that:

- (a) every dispatched instruction passes the **pre-execution authorization checkpoint (Gate A · EXEC_AUTH)** before physical execution begins on the target substrate;
- (b) no physical substrate can complete without producing a signed receipt at the **post-execution retirement checkpoint (Gate B · RETIRE)**; and
- (c) no P6-A/P6-B/P6-C tagged result can influence any decision-tagged operation downstream (equation25). Machine-checked artefacts are archived to the same Base 8453 anchor chain the substrate uses in operation, so the verification is auditable end-to-end.

SVA Properties · v0.2 Canonical Form

The three canonical SVA safety properties written against the two-gate model.

Safety 1 EXECUTE $\Rightarrow$ EXEC_AUTH

No substrate may execute an instruction that has not received an EXEC_AUTH decision from the verified Deontic path at Gate A.

Safety 2 RETIRE $\Rightarrow$ VERIFY

No instruction may reach the architectural RETIRE checkpoint at Gate B without completing measurement and verification.

Safety 3 DECISION_USE(P6_RESULT) $\Rightarrow$ FALSE

No decision-tagged operation may consume a P6-A, P6-B, or P6-C tagged result unless the result has passed the appropriate non-research path (*i.e.* has been re-classified out of the RESEARCH epistemic class via the ALLOW gate). This preserves the epistemic-class check of Paper XVII Section 7 and Section 10.4 of this paper.

22.2. Physical-Substrate Self-Test

Each substrate P1 - P5 has a dedicated boot-time self-test. P1 mesh calibration measures every MZI's insertion loss and phase-shifter range and fails safe if any cell exceeds fabricated tolerance. P2 Ising engine self-test runs a known 32-spin MaxCut and checks against the known ground state. P3 reservoir self-test measures λ_1 on a known input signal and fails safe if outside the Section 7.4 trust region. P4 phononic self-test measures bandgap edges via a swept optical probe. P5 memris-

tor self-testwrites and reads a checkerboard pattern to every crossbar row. P6-A (if attached) self-tests the Casimir gap through capacitive readout and refuses to enable if calibration fails. P6-B and P6-C follow analogous laboratory-configuration self-tests.

22.3. Peer-Review Protocol

This v0.2 paper is intended for peer review as follows: (a) archival version submitted to ResearchGate under Paper XIX numbering, v0.2; (b) supplementary artefacts (RTL, SVA properties, EL-IR compiler, benchmark suite) archived to a public Base 8453 anchor and mirrored on Git Hub *Red Ciprian Pater/CHAINSTATE-X*; (c) SVA formal-verification archive released as an OSS repository under Apache-2.0; (d) benchmark reproduction kit provided to independent reviewers on request. Reviewers are asked to independently reproduce three benchmarks: (i) a 128×128 photonic MZI mesh linear transformation, (ii) a 256-spin fully-connected MaxCut convergence, (iii) a P3 reservoir time-series prediction on the Mackey-Glass benchmark. Reproduction failure on any of these constitutes falsification of the corresponding section's performance claims.

22.4. Falsification Criteria per Section · Updated for v0.2

Section	Substrate	Falsification threshold
Section 5	P1	MZI mesh insertion loss exceeds 12 dB end-to-end [9]
Section 6	P2	Ising coupling-matrix fidelity falls below 0.90 (relaxed from 0.986 target)
Section 7	P3	Reservoir stability trust region fails on Mackey-Glass benchmark (NRMSE ≥ 0.1) or $\hat{\lambda}_1 - u_{\lambda}$ exceeds $\lambda_{\text{fuse}} - \delta_{\lambda}$
Section 8	P4	Diamond phononic crystal bandgap fails to demonstrate 50 - 70 GHz
Section 9	P5	HfO2crossbar shows fewer than 104 distinct analog states
Section 10.1	P6-A	Casimir cavity Q or force-sensitivity fails to reproduce cited [16] envelope
Section 10.2	P6-B	DCE photon statistics fail to reproduce [19] Bogoliubov signature
Section 10.3	P6-C	Sonoluminescence spectrum fails to correlate with any CS.* classification (per programme criterion)
Section 18.1	TTS	End-to-end TTS at $q = 0.99$, $p^* = 0.99$ exceeds 100 μs on the 256-spin reference graph (matching best merchant competitor)

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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Appendix: CHAINSTATE-X Architecture Summary

The complete architecture spans seven physical layers L0 - L6 with a common CS.PHYSOPT ISA, an RV64GCexecutive, six parallel physical substrates P1 - P6, and a measurement + provenance chain that anchors every retired instruction to Base 8453.

Symbol	Meaning	Symbol	Meaning
λ	wavelength	T	temperature
φ	optical phase	B	magnetic field
p	polarisation	E	electric field
m	spatial mode	μ	chemical potential
t	temporal mode	ε	strain
d	cavity gap	J	coupling
κ	loss rate	Ω	drive frequency

Canonical state vector $\Lambda = (\lambda, \varphi, p, m, t, T, B, E, \mu, \varepsilon, d, J, \kappa, \Omega) \cdot 14$ scalar variables. Geometry is a derived configuration object rather than one of the fourteen scalar state variables. This corrects the earlier v0.1 Section 3.2, which enumerated 12 elements while claiming the same 14-variable list.