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An Assessment of an Overcurrent Protection Relay Tripping Time and Coordination at Pencawang Masuk Utama Jasin Melaka Using PSCAD Software

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Abstract

This study presents a PSCAD simulation model of the 132/11 kV Pencawang Masuk Utama (PMU) in Jasin, Melaka, designed to evaluate the performance of Inverse Definite Minimum Time (IDMT) overcurrent relays. The system was subjected to various fault scenarios, including three-phase bolted, standard three-phase, and double line-to-ground faults across different network locations to assess operating and coordination times. The analysis confirms that the relay response times align with theoretical expectations, verifying the reliability of the protection scheme.

Keywords

Overcurrent Relay, PSCAD, Pickup Current, Pencawang Masuk Utama, Time Multiplier Setting

1. Introduction

Modeling overcurrent protection for complex networks with a large number of busbars typically requires the use of PSCAD, as manual calculations often prove insufficient due to system complexity. The stability and dependability of the electrical grid rely heavily on protecting critical apparatus such as generators, transformers, and transmission lines from the destructive high currents associated with

short-circuit faults. Fundamentally, when the power system experiences abnormal conditions, protective relays must detect the fault current and trip the circuit breaker to prevent equipment damage. Consequently, electrical engineers utilize PSCAD to design and analyze power flow, as it provides a safe environment to simulate potential fault scenarios [1]-[3].

PSCAD is employed to analyze network current and voltage by simulating various fault conditions, including overloads and short circuits. This process estimates fault current values, which are essential for determining precise relay settings and coordination. Using simulation data, these settings can be tuned to optimize device coordination, ensuring the protection system operates at peak efficiency. This approach significantly contributes to the safety and reliability of electrical grids by preventing damage, maintaining power supply continuity, and enhancing overall system durability [4]-[6].

In summary, modeling overcurrent protection in PSCAD plays a pivotal role in power system design and analysis. It enables engineers to evaluate the performance of protection devices within a controlled, simulated environment, ensuring an effective response to fault currents.

The primary objective of this paper is to verify the two critical configuration parameters of the overcurrent relays at Pencawang Masuk Utama (PMU) Jasin: The Plug Setting Multiplier (PSM) and the Time Multiplier Setting (TMS). The study compares theoretically calculated PSM and TMS values against simulation results to validate that the protection scheme meets the essential requirements for both selectivity and sensitivity.

2. Methodology

The simulation models the network at Pencawang Masuk Utama (PMU) Jasin. This system operates at a primary voltage of 132 kV, which is stepped down via transformers to an 11kV network feeding Stesen Suis Utama (SSU) XINYI, Pencawang Pengagihan Utama (PPU) Selandar, and PPU Jasin Bestari (refer to **Figure 1**). This voltage is subsequently stepped down to low-voltage levels (400 V/230 V) for consumer distribution.

To ensure effective overcurrent protection, precise coordination of relay plug settings and time responses is critical. Consequently, the pickup current and Time Multiplier Setting (TMS) were calculated manually. The Plug Setting Multiplier (PSM) is defined by the following equation [7]-[10]:

$$\mathrm{PSM} = \mathrm{I\ relay}/\mathrm{PS} \tag{1}$$

where $\mathrm{I\ relay}$ represents the current flowing through the relay's operating coil, and PS denotes the plug setting of the relay. Furthermore, the relay's operating time is calculated based on the standard inverse characteristic curve, as expressed in the following equation [7]-[10]:

$$\mathrm{Top} = 0.14 * (\mathrm{TMS}) \Big/ \left(\mathrm{PSM}^{0.02} - 1\right) \tag{2}$$

where PSM represents the Plug Setting Multiplier and TMS denotes the Time Mul-

tiplier Setting. Table 1 summarizes the specific TMS and Plug Setting values configured for each relay in this simulation. Following the manual calculations, PSCAD software was employed to model the relay response. Example of setting Relay 8 is as follows:

Relay 8

I_{LOAD} has been determined in power flow network.

I_{LOAD} 8 = 1399.32 A

Choose CT = 1000/1 A

Plug Setting = I $_{LOAD}$ × 100

$I_{PRIMARY}$ CT = 1399.32 × 100/1000

= 139.93%

∴*Choose* 150% *as Plug Setting*

Relay 8, acting as the downstream unit, is designated as the primary protection for this fault. With a Time Multiplier Setting (TMS) of 0.1, the operation time (Top) is calculated using Equations (1) and (2). To evaluate performance, standard fault scenarios including three-phase-to-ground, double line, and double line-to-ground faults were simulated. The tripping sequence depends on the fault location; for instance, a three-phase fault at PPU Jasin Bestari triggers Relay 8 first, followed sequentially by Relays 7, 2, and 1, as illustrated in Figure 1.

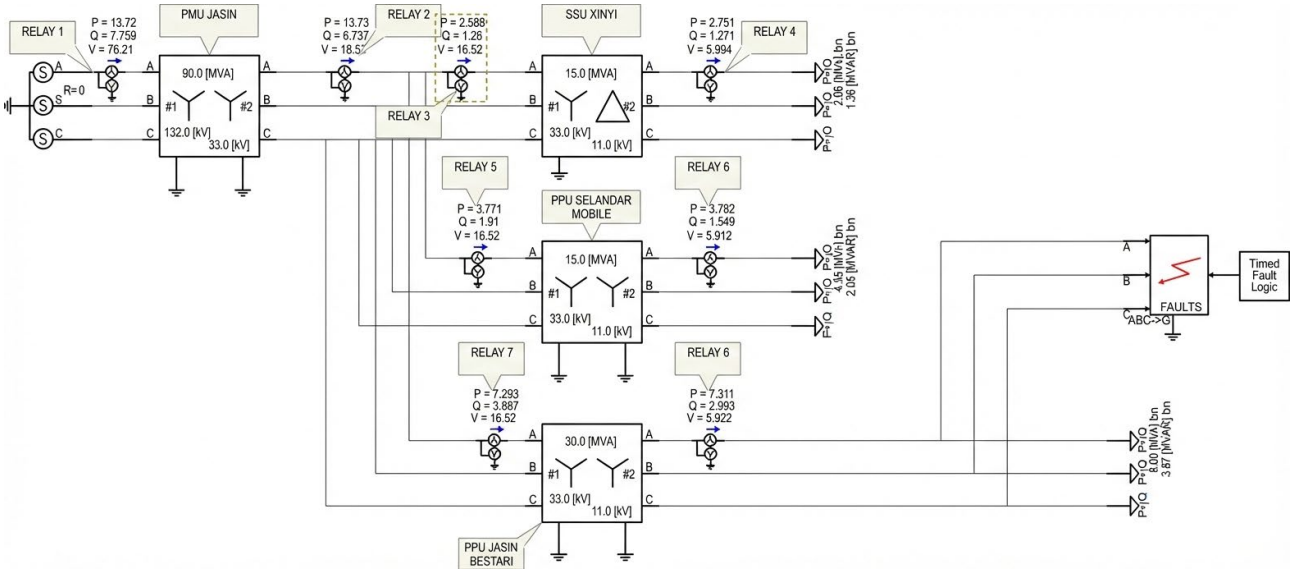


Figure 1. PMU Jasin network.

Table 1. Setting of overcurrent relay.

Relay	Plug setting	TMS	Curve type
Relay 1	100%	0.3732	Standard inverse
Relay 2	100%	0.2708	Standard inverse
Relay 3	100%	0.293	Standard inverse

Continued

Relay 4	75%	0.1206	Standard inverse
Relay 5	100%	0.2428	Standard inverse
Relay 6	100%	0.1031	Standard inverse
Relay 7	100%	0.2497	Standard inverse
Relay 8	150%	0.1	Standard inverse

3. Results and Discussion

The study simulates five distinct fault types across four critical network locations: PMU Jasin, PPU Jasin Bestari, SSU XinYi, and PPU Selandar Mobile. In each scenario, the discrimination time between relays is rigorously analyzed and discussed to ensure proper coordination around 0.5 s [7]-[10].

3.1. Case 1 (PPU Jasin Bestari)

3.1.1. LLLG Fault

A three-phase bolted fault was initiated at PPU Jasin Bestari to monitor the tripping response of each relay. The resulting operating times are detailed in Table 2.

Table 2. Relay operation time and discrimination of LLLG fault in Case 1.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	1018.29 A	2.3058 s	0.5002 s
Relay 2	4059.47 A	1.8056 s	0.4918 s
Relay 3	121.11 A	NO TRIPPING	-
Relay 4	361.14 A	NO TRIPPING	-
Relay 5	173.07 A	NO TRIPPING	-
Relay 6	516.49 A	NO TRIPPING	-
Relay 7	389.63 A	1.3138 s	0.499 s
Relay 8	11683.32 A	0.8148 s	-

Table 2 outlines the tripping sequence: Relay 8, followed by Relays 7, 2, and 1. Relay 8 functions as the primary protection, while the subsequent relays act as backup with a coordination interval of approximately 0.5 s.

The specific operating times demonstrate accurate grading:

Relay 8: Trips at 0.8148 s.

Relay 7: Trips at 1.3138 s (a 0.499 s delay).

Relay 2: Trips at 1.8056 s (a 0.4918 s delay relative to Relay 7).

Relay 1: Trips at 2.3058 s (a 0.5002 s delay relative to Relay 2).

Relays 3, 4, 5, and 6 remained stable and did not trip, as the fault was located outside their respective protection zones. These results confirm that the simulated operating times successfully meet the required discrimination time margins.

3.1.2. LLL Fault

A three-phase fault was simulated at PPU Jasin Bestari to evaluate the tripping response of each relay. The corresponding operating times are recorded in Table 3.

Table 3. Relay operation time and discrimination of LLL fault in Case 1.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	1017.52 A	2.2368 s	0.5003 s
Relay 2	4056.41 A	1.7365 s	0.4707 s
Relay 3	121.11 A	NO TRIPPING	-
Relay 4	361.15 A	NO TRIPPING	-
Relay 5	173.07 A	NO TRIPPING	-
Relay 6	516.46 A	NO TRIPPING	-
Relay 7	3897.32 A	1.2658 s	0.4745 s
Relay 8	11686.11	0.7913 s	-

As shown in Table 3, the relays trip in the following sequence: Relay 8, Relay 7, Relay 2, and Relay 1. These simulated operating times confirm that the system maintains the required discrimination time margins between each protection stage.

3.1.3. LLG Fault

A double line-to-ground fault was initiated at PPU Jasin Bestari to evaluate the tripping response of each relay. The recorded operating times are detailed in Table 4.

Table 4. Relay operation time and discrimination of LLG fault in Case 1.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	1020.60 A	2.303 s	0.4997 s
Relay 2	4068.72 A	1.8035 s	0.4893 s
Relay 3	126.82 A	NO TRIPPING	-
Relay 4	415.38 A	NO TRIPPING	-
Relay 5	172.93 A	NO TRIPPING	-
Relay 6	516.08 A	NO TRIPPING	-
Relay 7	3893.38 A	1.3142 s	0.499 s
Relay 8	11674.30 A	0.8148 s	-

Table 4 demonstrates a correct tripping order of Relay 8, Relay 7, Relay 2, and Relay 1. The results verify that the operation times fall within the specified discrimination ranges, ensuring effective system protection.

3.2. Case 2 (SSU XinYi)

3.2.1. LLLG Fault

A three-phase bolted fault is applied at the SSU XinYi and tripping time at each relay has been observed. Table 5 shows the relay operating time.

Table 5. Relay operation time and discrimination of LLLG fault in Case 2.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	641.85 A	3.1716 s	0.7426 s
Relay 2	2553.17 A	2.429 s	1.1307 s
Relay 3	2205.35 A	1.2983 s	0.4815 s
Relay 4	6612.64 A	0.8168 s	-
Relay 5	195.87 A	NO TRIPPING	-
Relay 6	584.52 A	NO TRIPPING	-
Relay 7	378.18 A	NO TRIPPING	-
Relay 8	1128.40 A	NO TRIPPING	-

As indicated in Table 5, the relays trip in the sequence of Relay 4, Relay 3, Relay 2, and Relay 1. A comparison between Case 1 and Case 2 reveals a significant reduction in fault currents for Relays 1 and 2 in the latter, attributed to the lower load in Case 2. Due to the inverse current-time characteristic, this reduced fault current results in a longer operating time for Relays 1 and 2 in Case 2 compared to Case 1.

3.2.2. LLL Fault

A three-phase fault is applied at SSU XinYi and tripping time at each relay has been observed. Table 6 shows the relay operating time.

Table 6. Relay operation time and discrimination of LLL fault in Case 2.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	641.05 A	3.016 s	0.7415 s
Relay 2	2549.95 A	2.2745 s	1.0307 s
Relay 3	2205.62 A	1.2438 s	0.4403 s
Relay 4	6613.27 A	0.8035 s	-
Relay 5	195.87 A	NO TRIPPING	-
Relay 6	584.53 A	NO TRIPPING	-
Relay 7	378.20 A	NO TRIPPING	-
Relay 8	1128.42 A	NO TRIPPING	-

Table 6 indicates a tripping sequence of Relay 4, Relay 3, Relay 2, and Relay 1. However, the observed discrimination times do not strictly align with the standard grading margins. This deviation occurs because Relays 1 and 2 are configured

based on Case 1 (the worst-case fault scenario). Despite this discrepancy in grading margins, the relays successfully maintain the correct tripping sequence and isolate the fault as expected.

3.2.3. LLG Fault

A line-to-line-to-ground fault is applied at the SSU XinYi and tripping time at each relay has been observed. Table 7 shows the relay operating time.

Table 7. Relay operation time and discrimination of LLG fault in Case 2.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	641.83 A	3.1715 s	0.7425 s
Relay 2	2553.11 A	2.429 s	1.1307 s
Relay 3	2205.33 A	1.2983 s	0.496 s
Relay 4	6024.18 A	0.8203 s	-
Relay 5	195.86 A	NO TRIPPING	-
Relay 6	584.51 A	NO TRIPPING	-
Relay 7	378.17 A	NO TRIPPING	-
Relay 8	1128.37 A	NO TRIPPING	-

Consistent with previous scenarios, Table 7 shows a tripping sequence of Relay 4, Relay 3, Relay 2, and Relay 1. The discrimination times in this simulation do not strictly adhere to the standard grading margins. This deviation is expected, as Relays 1 and 2 utilize fixed settings derived from Case 1 (the worst-case fault scenario). Nevertheless, the relays operate successfully and maintain the required protection sequence.

3.3. Case 3 (PPU SELANDAR MOBILE)

3.3.1. LLLG Fault

A three-phase bolted fault is applied at the PPU SELANDAR MOBILE and tripping time at each relay has been observed. Table 8 shows the relay operating time.

Table 8. Relay operation time and discrimination of LLLG fault in Case 3.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	632.80 A	3.2142 s	0.7534 s
Relay 2	2516.92 A	2.4608 s	1.168 s
Relay 3	137.36 A	NO TRIPPING	-
Relay 4	409.48 A	NO TRIPPING	-
Relay 5	2210.14 A	1.2928 s	0.4905 s
Relay 6	6627.11 A	0.8023 s	-
Relay 7	379.01 A	NO TRIPPING	-
Relay 8	1130.85 A	NO TRIPPING	-

As indicated in Table 8, the relays operate in the following sequence: Relay 6, Relay 5, Relay 2, and Relay 1. However, it is observed that the discrimination time falls outside the specified range in this scenario.

3.3.2. LLL Fault

A three-phase fault is applied at the PPU SELANDAR MOBILE and tripping time at each relay has been observed. Table 9 shows the relay operating time.

Table 9. Relay operation time and discrimination of LLL fault in Case 3.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	632.06 A	3.0583 s	0.7526 s
Relay 2	2513.94 A	2.305 s	1.0752 s
Relay 3	137.36 A	NO TRIPPING	-
Relay 4	409.51 A	NO TRIPPING	-
Relay 5	2210.37 A	1.2305 s	0.4458 s
Relay 6	6627.78 A	0.7847 s	-
Relay 7	379.02 A	NO TRIPPING	-
Relay 8	11308.80 A	NO TRIPPING	-

As demonstrated in Table 9, the relays trip in the sequence of Relay 6, Relay 5, Relay 2, and Relay 1. However, the observed discrimination times fall outside the acceptable range for this scenario.

3.3.3. LLG Fault

A line-to-line-to-ground fault is applied at the PPU SELANDAR MOBILE and tripping time at each relay has been observed. Table 10 shows the relay operating time.

Table 10. Relay operation time and discrimination of LLG fault in Case 3.

Relay	Fault current	Tripping time	Discrimination time
Relay 1	634.24 A	3.2078 s	0.7515 s
Relay 2	2522.66 A	2.4563 s	1.1636 s
Relay 3	140.35 A	NO TRIPPING	-
Relay 4	439.46 A	NO TRIPPING	-
Relay 5	2209.19 A	1.2927 s	0.4902 s
Relay 6	6624.26 A	0.8025 s	-
Relay 7	378.83 A	NO TRIPPING	-
Relay 8	1130.34 A	NO TRIPPING	-

Table 10 indicates a tripping sequence of Relay 6, Relay 5, Relay 2, and Relay 1. Similar to previous cases, the observed discrimination times do not strictly follow the standard grading margins. This occurs because Relays 1 and 2 retain the settings op-

timized for Case 1 (the worst-case fault scenario). Despite this deviation in timing, the relays continue to trip reliably and maintain the expected protection sequence.

4. Case 4 (PMU Jasin)

The simulation results for all types of faults at PMU Jasin are shown in Tables 11-13 respectively.

Table 11. Relay operation time and discrimination (lllg fault).

Relay	Fault current	Tripping time	Discrimination time
Relay 1	3937.16 A	1.3793 s	0.251 s
Relay 2	15740.75 A	1.1283 s	-
Relay 3	1.35 A	NO TRIPPING	-
Relay 4	19.08 A	NO TRIPPING	-
Relay 5	1.93 A	NO TRIPPING	-
Relay 6	5.79 A	NO TRIPPING	-
Relay 7	3.72 A	NO TRIPPING	-
Relay 8	11.10 A	NO TRIPPING	-

Table 12. Relay operation time and discrimination (lll fault).

Relay	Fault current	Tripping time	Discrimination time
Relay 1	3939.21 A	1.3242 s	0.2334 s
Relay 2	15749 A	1.0908 s	-
Relay 3	2.54 A	NO TRIPPING	-
Relay 4	13.46 A	NO TRIPPING	-
Relay 5	2.67 A	NO TRIPPING	-
Relay 6	7.81 A	NO TRIPPING	-
Relay 7	8.89 A	NO TRIPPING	-
Relay 8	26.27 A	NO TRIPPING	-

Table 13. Relay operation time and discrimination (llg fault).

Relay	Fault current	Tripping time	Discrimination time
Relay 1	3937.46 A	1.3793 s	0.2513 s
Relay 2	15741.83 A	1.128 s	-
Relay 3	54.38 A	NO TRIPPING	-
Relay 4	277.14 A	NO TRIPPING	-
Relay 5	2 A	NO TRIPPING	-
Relay 6	5.97 A	NO TRIPPING	-
Relay 7	150.04 A	NO TRIPPING	-
Relay 8	447.67 A	NO TRIPPING	-

In all cases, it is clear that Relay 2 and Relay 1 will trip accordingly. Moreover, the discrimination time is out of range due to Relay 2 and Relay 1 settings. However, the relays are still tripping as expected in these cases.

5. Conclusion

To summarize, the study verified the relay settings under various fault conditions using PSCAD. While the discrimination times showed slight variance from the theoretical range, the relays proved effective by successfully tripping for Three-Phase (LLL), Three-Phase-to-Ground (LLLG), and Double Line-to-Ground (LLG) faults at multiple locations. These results demonstrate that the overcurrent relays provide reliable protection and uphold system stability.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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