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Realization of Resistorless Voltage Mode Universal Filter and Quadrature Oscillator Employing DDTAs with CMOS 180 nm Technology at 0.2 V

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Abstract

This paper presents a low-supply-voltage CMOS realization of a Differential Difference Transconductance Amplifier (DDTA) operating at a supply voltage of 0.2 V. The proposed DDTA achieves high operational capability while consuming ultra-low power of 356.66 nW, making it suitable for low-frequency biomedical and sensor applications. The proposed configuration employs two DDTAs and two grounded capacitors to implement a voltage-mode universal filter and a quadrature oscillator. These circuits are applicable to signal generation, audio and image processing, instrumentation, biomedical systems, and sensor interfaces. The universal filter exhibits high input impedance and allows electronic tuning of the natural frequency in the range of a few hundred hertz. The band-pass filter demonstrates a total harmonic distortion (THD) of 0.46% for a 100 mVpp input signal at a frequency of 83.97 Hz. With minor modifications to the universal filter structure, a quadrature oscillator is obtained in which both the condition of oscillation and the oscillation frequency are electronically controllable. The THD corresponding to an oscillation frequency of 68.23 Hz is approximately 1.16%. The proposed circuits are designed and simulated using 180 nm CMOS technology in PSPICE. Simulation results confirm the effectiveness and performance of the proposed universal configuration.

Keywords

CMOS Technology, Differential Difference Transconductance Amplifier (DDTA), Voltage Mode Universal Filter, Quadrature Oscillator

1. Introduction

In the present era, researchers and academicians are increasingly focused on achieving extremely low-voltage operation and ultra-low power consumption, which have become inevitable requirements for modern battery-operated portable electronic equipment and self-powered systems. In advanced nanoscale complementary metal-oxide-semiconductor (CMOS) technologies, scaling down the power supply voltage enhances the reliability and performance of digital circuits; however, it leads to significant performance degradation in analog circuits and active devices. This creates continuous challenges for analog circuit designers in maintaining acceptable performance for practical applications and system-on-chip (SoC) designs. The primary effects of supply voltage reduction on analog circuits, such as operational amplifiers (op-amps) and operational transconductance amplifiers (OTAs), include reduced input voltage swing, lower transconductance, and diminished voltage gain. Conventional techniques to enhance input voltage swing employ rail-to-rail architectures using both PMOS and NMOS differential pairs. Although effective, these approaches increase circuit complexity due to the inclusion of additional differential pairs, current branches, and auxiliary circuitry required to maintain constant transconductance over the entire input voltage swing range. Over the last two decades, extensive research efforts have been reported on the design of universal filters and quadrature oscillators using various modern analog building blocks (BBs), such as Recent research has demonstrated significant progress in the development of universal filters, oscillators, and low-voltage analog circuits using various active building blocks. VDGA-based resistorless mixed-mode universal filters with dual-mode quadrature oscillation capability were reported in [1], while cascadeable single-input multiple-output inverse filter configurations were introduced in [2]. First-order VM/TAM universal filters employing a single-differential difference current conveyor were investigated along with their applications in [3]. The practical feasibility of on-chip biquadratic filters and oscillators was experimentally validated in [4]. Furthermore, first-order universal active filters were developed by extending two-CFOA-GC all-pass filter structures [5]. Research on low-voltage and energy-efficient filter architectures includes 0.5-V nano-power voltage-mode first-order universal filters using multiple-input OTAs [6] and a highly linear 0.3-V rail-to-rail bulk-driven OTA implemented in 0.13-μm CMOS technology [7]. A first-order universal filter based on two ICCII+s and a grounded capacitor was proposed in [8], whereas electronically controllable voltage-mode multifunction filters implemented using commercially available ICs were presented in [9]. SITO voltage-mode multifunction biquad filters with electronic and orthogonal tuning capabilities using LT1228 devices were investigated in [10]. A synthesis approach employing two VD-DIBAs was proposed to achieve independent tuning of the quality factor and natural frequency [11]. VDBA-based mixed-mode universal filters with enhanced high-Q controllability were reported in [12]. CMOS implementations of electronically tunable filters based on VDCC and VDTA structures were subsequently presented

in [13] and [14], respectively. Fully electronically tunable first-order all-pass filters using VDVTA and OTA architectures were also demonstrated at a supply voltage of ±0.85 V [15]. In addition, current-mode first-order universal filters and their corresponding voltage-mode transformation were investigated in [16]. Supplementary CCII-based second-order universal filters and quadrature oscillators were presented in [17], while voltage-mode multifunction biquad filters incorporating fully uncoupled quadrature oscillator configurations were reported in [18]. To support the implementation of low-voltage analog systems, a 0.3-V differential difference amplifier was developed in [19], and sub-0.5-V operational transconductance amplifiers were realized in 0.18-μm CMOS technology in [20].

2. Description of DDTA and Its CMOS Realization Structure

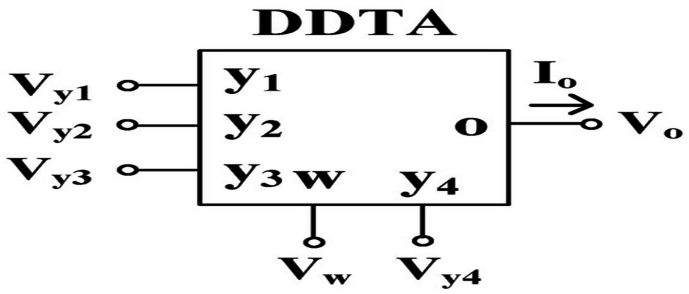

Figure 1. Symbolic representation of DDTAs.

The symbolical representation of the DDTA is reported in **Figure 1**. The Differential Difference Transconductance Amplifier (DDTA) is a versatile analog building block widely used in filter applications. Its applications also extend to communication, control, instrumentation, and biomedical systems. In such applications, biquadratic filters and oscillators are commonly employed, where low supply voltage operation and low power consumption are critical design requirements. The DDTA combines the advantageous features of a Differential Difference Amplifier (DDA), such as unity-gain voltage addition and subtraction, high input impedance, and a reduced number of components, with the benefits of an Operational Transconductance Amplifier (OTA), including electronic tunability and simple circuit implementation. This combination makes the DDTA an efficient and flexible solution for low-voltage, low-power analog signal-processing applications. Ideal characteristics of DDTA is described by the following Equations (1) and (2):

$$V_W = V_{Y1} + V_{Y3} - V_{Y2} \tag{1}$$

$$I_0 = g_m \left(V_W - V_{Y4} \right) \tag{2}$$

The CMOS structure of the proposed DDTA is shown in **Figure 2**. The configuration consists of two main active building blocks: a differential-difference amplifier operating in a unity-feedback configuration, thereby forming a differential-difference current conveyor (DDCC), and a transconductance amplifier. Both

building blocks are based on non-tailed differential amplifier architectures, which enable ultra-low-voltage operation while providing a rail-to-rail input voltage swing. The DDCC building block comprises two stages: an input differential amplifier formed by transistors M_1 - M_6, followed by a class-A output stage implemented using MOS transistors M_9 - M_{10}. Frequency compensation is achieved using the compensation capacitor CCC_CCC, whose value can be determined using the same design principles applied to a conventional two-stage operational amplifier. The input stage of the DDCC circuit can be presented as a non-tailed differential pair with an additional partial positive feedback circuit.

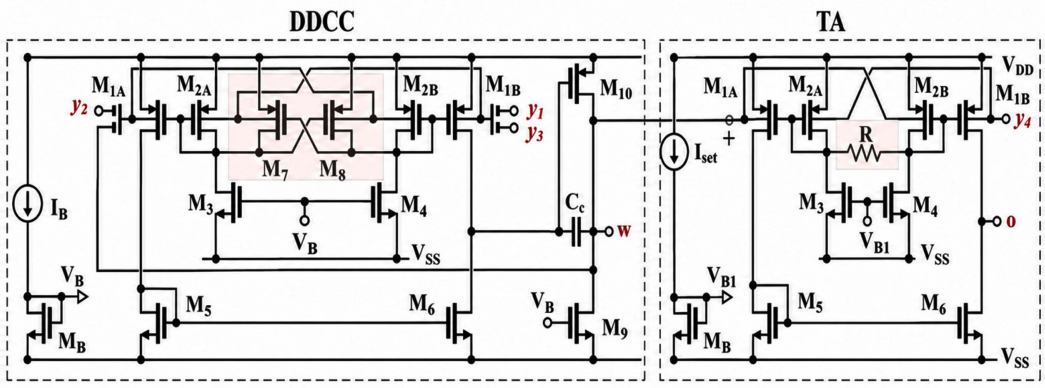

Figure 2. CMOS realization of DDTA.

Transistors M_7 and M_8 introduce negative conductances of $-g_{m7}$ and $-g_{m8}$ respectively, which counteract the positive conductances of the diode-connected transistors $M_{2A,B}$ (approximately g_{m2}). This interaction increases the effective resistance at the gate-drain nodes, leading to an improvement in voltage gain between the input terminals and the gate nodes of $M_{1A,B}$. Consequently, the first stage exhibits enhanced transconductance and voltage gain. In the proposed architecture, the input transistors $M_{1A,B}$ are realized using bulk-driven multiple-input MOST (MI-MOST) devices. This implementation reduces circuit complexity and lowers overall power consumption by removing an additional differential stage commonly found in conventional DDCC designs. The summation of input signals is accomplished using a capacitive voltage-summing network, eliminating the need for extra active circuitry. Large-valued MOS resistances are connected in parallel with these capacitors to provide proper DC biasing for the bulk-driven MI-MOST transistors. These resistive elements are implemented using anti-parallel MOS transistors operating in the cutoff region.

3. Proposed Applications of DDTA

3.1. Proposed Voltage-Mode MIMO Universal Filter

The proposed voltage-mode multiple-input multiple-output (MIMO) universal filter configuration, implemented using the DDTA, is illustrated in Figure 3. The circuit employs two DDTAs and two grounded capacitors. The input nodes V_{in1},

V_{in2}, V_{in3}, V_{in4}, and V_{in5} exhibit high input impedance, making the configuration suitable for voltage-mode signal processing. Output nodes V_{o1} and V_{o3} provide low output impedance, whereas output nodes V_{o2} and V_{o4} require additional buffering when driving low-impedance loads in the proposed configuration.

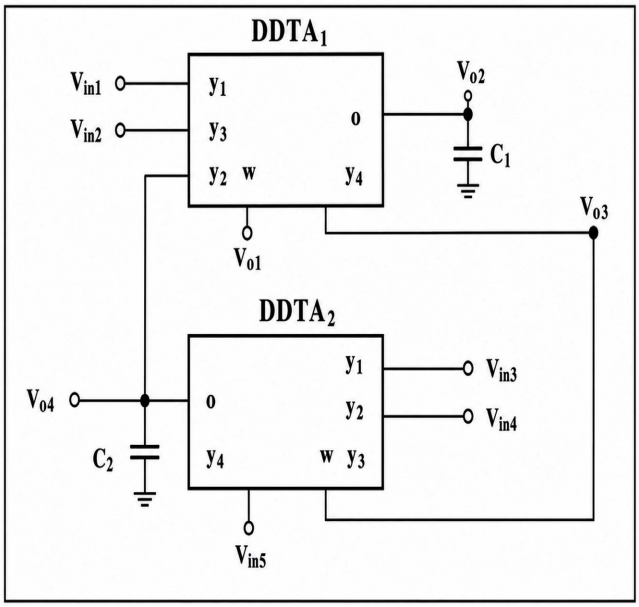

Figure 3. Proposed resistorless MIMO universal filter employing DDTAs.

The theoretical analysis of MIMO universal filter configuration presented in Figure 3. The equations for the output voltages can be presented by the following Equations (3)-(6) respectively are as follows:

$$V_{o1} = \frac{(V_{in1}+V_{in2})\left(S^2C_1C_2 + SC_2g_{m1}\right) + (V_{in3}-V_{in4})SC_1g_{m2} + V_{in5}\left(SC_1g_{m2} + g_{m1}g_{m2}\right)}{S^2C_1C_2 + SC_2g_{m1} + g_{m1}g_{m2}} \quad (3)$$

$$V_{o2} = \frac{(V_{in1}+V_{in2})SC_2g_{m1} + \left(SC_2g_{m1} + g_{m1}g_{m2}\right)(V_{in3}-V_{in4})SC_1g_{m2} - V_{in5}g_{m1}g_{m2}}{S^2C_1C_2 + SC_2g_{m1} + g_{m1}g_{m2}} \quad (4)$$

$$V_{o3} = \frac{g_{m1}g_{m2}(V_{in1}+V_{in2}) + (V_{in4}-V_{in3})SC_1g_{m2} - \left(SC_1g_{m2} - g_{m1}g_{m2}\right)V_{in5}}{S^2C_1C_2 + SC_2g_{m1} + g_{m1}g_{m2}} \quad (5)$$

$$V_{o4} = \frac{(V_{in1}+V_{in2})g_{m1}g_{m2} + SC_1g_{m2}(V_{in4}-V_{in3}) - \left(SC_1g_{m2} + g_{m1}g_{m2}\right)V_{in5}}{S^2C_1C_2 + SC_2g_{m1} + g_{m1}g_{m2}} \quad (6)$$

Natural frequency (ω_0) and the quality factor (Q) of the Voltage Mode Universal filter can be presented in Equation (7), (8) respectively are as follows:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (7)$$

$$Q_0 = \sqrt{\frac{C_1g_{m2}}{g_{m1}C_2}} \quad (8)$$

From (7) and (8), the natural frequency and the quality factor can be designed,

as the quality factor can be given by the proper selection $\frac{C_1}{C_2}$ with $g_{m1} = g_{m2}$ whereas the natural frequency can be obtained electronically tunable by $g_{m1} = g_{m2} = g_m$.

3.2. Proposed Application as a Voltage-Mode MIMO Quadrature Oscillator

The proposed voltage mode MIMO Quadrature Oscillator Configuration as an application of DDTA. It employs two DDTAs and two grounded capacitors. The proposed universal filter in Figure 3 is modified to work as a quadrature oscillator as reported in Figure 4. It can be obtained by using a non-inverting Band Pass filtering response and a feedback connection.

The transfer function of the Proposed Resistorless Quadrature Oscillator Employing DDTAs between V_{o1} and V_{in3} can be characterized by Equation (9) are as follows:

$$\frac{V_{o1}}{V_{in3}} = \frac{SC_1 g_{m2}}{S^2 C_1 C_2 + SC_2 g_{m1} + g_{m1} g_{m2}} \tag{9}$$

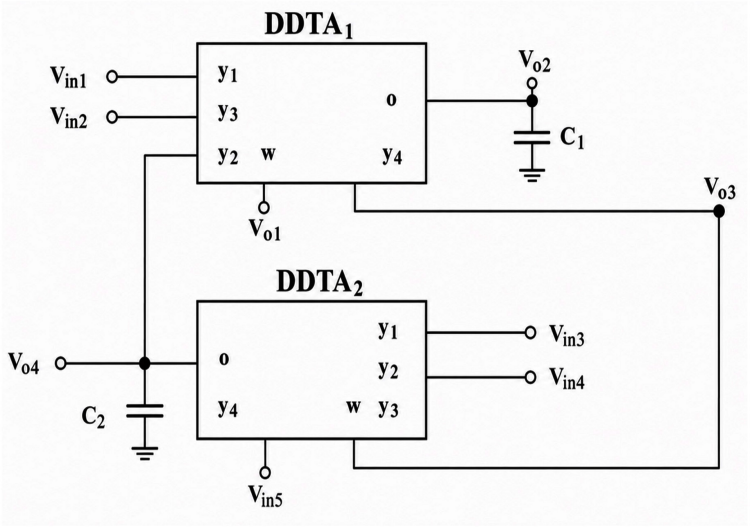

Figure 4. Proposed resistorless quadrature oscillator employing DDTAs.

The transfer function of the Proposed Resistorless Quadrature Oscillator Employing DDTAs unity between V_{o1} and V_{in3} can be characterized in Equation (10) as follows:

$$\frac{V_{o1}}{V_{in3}} = 1 \tag{10}$$

The Characteristic Equation of the Proposed Resistorless Quadrature Oscillator Employing DDTAs can be presented in Equation (11) are as:

$$S^2 C_1 C_2 + S\left(C_2 g_{m1} - C_1 g_{m2}\right) + g_{m1} g_{m2} = 0 \tag{11}$$

Condition of Oscillation can be presented in Equation (12) are as:

$$S\left(C_2 g_{m1} - C_1 g_{m2}\right) = 0 \tag{12}$$

$g_{m1} = g_{m2} = g_m$ and $C_2 = C_1$.

Frequency of Oscillation can given by the Equation (13)

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{13}$$

Frequency of Oscillation can be electronically controlled by the selection $g_{m1} = g_{m2} = g_m$ and $C_2 = C_1$.

The nodes V_{o3} and V_{o4} presents quadrature output signals. It can be confirmed from Equation (14) by the relationship between V_{o3} and V_{o4}

$$\frac{V_{o4}}{V_{o3}} = \frac{g_{m2}}{SC_2} \tag{14}$$

Therefore the phase difference between V_{o3} and V_{o4} is 90˚.

4. Non Ideal Effects

The non ideal characteristics of the DDTA are considered in the analysis of the proposed universal filter configuration which is reported in **Figure 3**, with particular emphasis on the non ideal behavior of the transconductance. Parasitic impedances are neglected, as the proposed circuit operates at low frequencies typically in biomedical signal processing. Under non-ideal conditions, the voltage V_W, output current I_0 and non ideal transconductance $g_{mni}(s)$ can be expressed by the Equations (15)-(17) respectively.

$$V_W = \beta_{i1} V_{y1} - \beta_{i2} V_{y2} + \beta_{i3} V_{y3} \tag{15}$$

$$I_0 = g_{mni}\left(V_W - V_{Y4}\right) \tag{16}$$

$$g_{mni}(s) \cong g_{mi}\left(1 - \mu_{is}\right) \tag{17}$$

where $\mu_i = \frac{1}{\omega_{gi}}$, ω_{gi} denotes the first order pole.

The output voltages of the proposed VM Universal Filter configuration can be described by Equations (18)-(21) respectively.

$$V_{o1} = \frac{\left(V_{in1}\beta_{11} + \beta_{13}V_{in2}\right)\left(S^2 C_1 C_2 + SC_2 g_{m1}\beta_{21}\right) + \left(\beta_{22}V_{in3} - \beta_{23}V_{in4}\right)SC_1 g_{m2}\beta_{12} + V_{in5}\left(SC_1 g_{m2}\beta_{12} + \beta_{12}\beta_{21}g_{m1}g_{m2}\right)}{S^2 C_1 C_2 + SC_2 g_{m1}\beta_{21} + g_{m1}g_{m2}\beta_{12}\beta_{21}} \tag{18}$$

$$V_{o2} = \frac{\left(V_{in1}\beta_{11} + \beta_{13}V_{in2}\right)SC_2 g_{mn1} + \left(\beta_{22}V_{in3} - \beta_{23}V_{in4}\right)\left(SC_2 g_{mn1} + g_{mn1}g_{mn2}\beta_{12}\right) - V_{in5}g_{mn1}g_{mn2}}{S^2 C_1 C_2 + SC_2 g_{m1}\beta_{21} + g_{m1}g_{m2}\beta_{12}\beta_{21}} \tag{19}$$

$$V_{o3} = \frac{S^2 C_2 C_2\left(V_{in4}\beta_{23} - V_{in3}\beta_{22}\right) + \left(V_{in1}\beta_{11} + V_{in2}\beta_{13}\right)SC_2 g_{mn1}\beta_{21} + V_{in5}g_{mn1}g_{mn2}\beta_{12}\beta_{21}}{S^2 C_1 C_2 + SC_2 g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{20}$$

$$V_{o4} = \frac{\left(V_{in1}\beta_{11} + \beta_{13}V_{in2}\right)\beta_{21}g_{mn1}g_{mn2} + SC_1 g_{mn2}\left(\beta_{23}V_{in4} - \beta_{22}V_{in3}\right) - \left(SC_1 g_{mn2} + \beta_{21}g_{mn1}g_{mn2}\right)V_{in5}}{S^2 C_1 C_2 + SC_2 g_{mn1}\beta_{21} + g_{mn1}g_{mn2}\beta_{12}\beta_{21}} \tag{21}$$

Natural frequency (ω_0) and the quality factor (Q_0) of the Voltage Mode Uni-

versal filter can be presented the Equations (22)-(23) respectively.

$$\omega_0 = \sqrt{\frac{g_{mn1}g_{mn2}\beta_{12}\beta_{21}}{C_1C_2}} \tag{22}$$

$$Q_0 = \sqrt{\frac{C_1 g_{mn2}\beta_{12}}{C_2 g_{mn1}\beta_{21}}} \tag{23}$$

where β_{i1} presents the voltage gain from V_{y1} to V_w of i-th DDTA, β_{i2} presents the voltage gain from V_{y2} to V_w of ith DDTA, and β_{i3} also denotes the voltage gain from V_{y2} to V_w of ith DDTA. Ideally, the voltage gains β_{i1}, β_{i2}, and β_{i3} are unity. The g_{mni} is the non-ideal transconductance gain of the DDTA, whose frequency dependence is given by parasitic capacitance C_o and resistance R_o at o-terminal. In the frequency range near the cutoff frequency, g_{mni} can be determined.

Modified Characteristics equation of the Quadrature Oscillator (24) can be described as

$$S^2C_1C_2 + \left(SC_2g_{gmn1}\beta_{21} - SC_1g_{mn2}\beta_{12}\beta_{22}\right) + g_{gmn1}g_{mn2}\beta_{12}\beta_{21} = 0 \tag{24}$$

Modified Characteristics equation of CO and FO for the Quadrature Oscillator (25) and (26) can be described as

$$SC_2g_{gmn1}\beta_{21} - SC_1g_{mn2}\beta_{12}\beta_{22} = 0 \tag{25}$$

Therefore $C_1\beta_{12}\beta_{22} = C_2\beta_{21}$

$$\omega_0 = \sqrt{\frac{g_{mn1}g_{mn2}\beta_{12}\beta_{21}}{C_1C_2}} \tag{26}$$

Since this work is mainly focused on circuits that operates at low frequency, Equation (26) is not taken in consideration. In the case that the universal filter and the quadrature oscillator operate in the frequency range in which the frequency dependence of g_m yields its influence, then (26) should be used to refine the error analysis.

5. Simulation Results

The proposed circuit was designed and simulated in PSPICE using 180 nm TSMC CMOS technology. A low supply voltage of 0.2 V was employed, while the bias current range of the DDTA was set in the range of 36.87 nA to 40 nA. The nominal setting current of the transconductance amplifier was chosen between 5 nA and 10 nA. Under the reported bias current range, the DDTA exhibits a power consumption ranging from 236 nW to 356.66 nW. The complete configuration was also implemented and verified using PSPICE with the same 180 nm CMOS technology. The aspect ratios of the MOS transistors used in the design are listed in Table 1. The circuit operates with a symmetrical supply voltage of 0.20 V, where V_{DD} = +0.10 V and V_{SS} = −0.10 V. The bias current of the DDCC varies from 46.77 nA to 49.88 nA, and the nominal setting current of the transconductance amplifier is fixed at Iset = 500 nA. The nominal power consumption of the DDTA is 356.66

nW, 69.78 nW consumed by the DDCC and 286.54 nW by the transconductance amplifier. When the setting current Iset is reduced to the bias current range from 5 nA to 10 nA, the simulated power consumption drops to 18.14 nW. This ultra-low power operation demonstrates the efficiency of the proposed design, making it highly suitable for battery-powered and energy-sensitive applications.

Table 1. MOS transistors aspect ratios of DDTA.

S. No	MOS Transistors	W (μm)/L (μm)
1.	M_{1A}, M_{1B}, M_{2A}, M_{2B}	20/3
2.	M_7 - M_8	15/3
3.	M_3 - M_6, M_B	10/3
4.	M_9	60/3
5.	M_{10}	120/3
6.	M_R	5/3

The simulated magnitude characteristics of the DDCC are presented in **Figure 5**. The simulated low-frequency gain for $V_W/V_{Y1} = V_W/V_{Y3}$ and V_W/V_{Y2} is 13.93 mdB and 58.21 mdB, while the −3 dB bandwidth is 21.67 kHz and 22.43 kHz, respectively. The DDCC enjoys rail to rail operation for all its inverting and non inverting input signals. This rail-to-rail operation capability is a design achievement for proposed configuration.

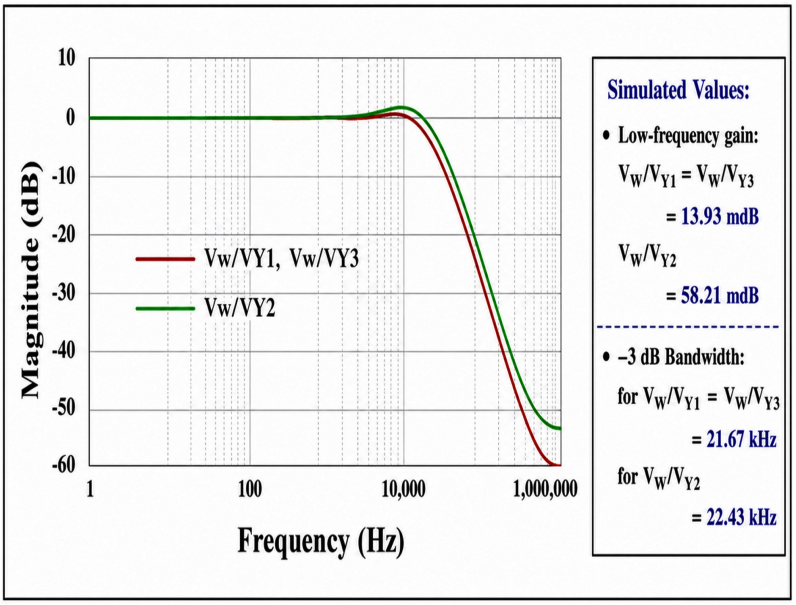

Figure 5. The simulated magnitude characteristics of the DDCC.

The simulated open-loop gain of the DDCC is presented in **Figure 6** (*i.e.*, without the unity gain feedback) which is simulated as 73.9 dB, and the phase margin is varied 55.76˚ - 56.19˚ for 10 pF to 20 pF load capacitor.

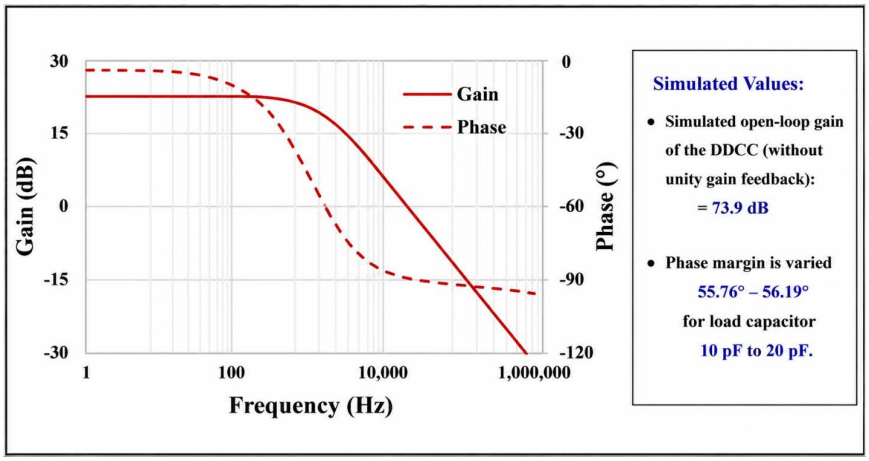

Figure 6. Simulated gain and phase response of the TA.

The multiple-input multiple-output (MIMO) universal filter configuration shown in the figure was simulated using off-chip capacitors with values $C_1 = C_2 =$ 5 nF. The magnitude responses corresponding to the low-pass (LPF), high-pass (HPF), band-pass (BPF), band-stop (BSF), and all-pass (APF) filters are illustrated in the figure. The simulated natural frequency (f_0) varies within the range of 81.59 Hz to 84.37 Hz. It is observed that the attenuation of the HPF and BPF responses deteriorates at very low frequencies. This behavior is primarily attributed to the finite output resistance of the transconductance amplifier, which is approximately 5.12 MΩ. For applications requiring improved attenuation characteristics, the output resistance can be enhanced by employing the MOS transistor self-cascode technique.

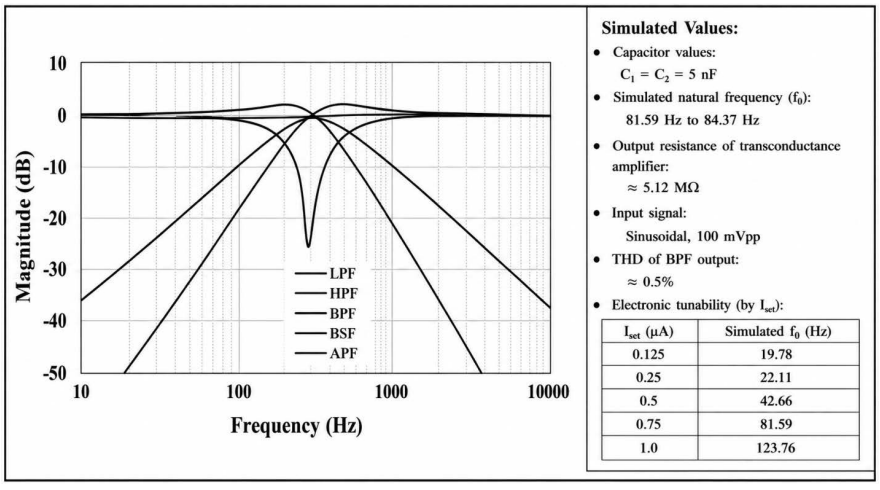

Figure 7. Simulated magnitude of various filtering for MIMO universal filter configuration.

The simulated filtering responses of the proposed voltage-mode DDTA-based universal filter are obtained by appropriately selecting the input signals, as summarized in Table 2. The performance of the multiple-input multiple-output (MIMO) universal filter is evaluated by applying a sinusoidal input signal with an

amplitude of 100 mVpp. The corresponding simulated natural frequency varies in the range of 81.59 Hz to 84.37 Hz. Under these conditions, the band-pass filter (BPF) output exhibits a total harmonic distortion (THD) of approximately 0.5%. Figure 7 illustrates the simulated filtering responses and electronic tunability of the low-pass (LPF), band-pass (BPF), high-pass (HPF), band-stop (BSF), and all-pass (APF) characteristics for different bias current settings. The tuning is achieved by varying the transconductance setting current Iset to 0.125 μA, 0.25 μA, 0.5 μA, and 0.75 μA, 1.0 μA. As a result, the simulated natural frequency (f_0) shifts to 19.78 Hz, 22.11 Hz, 42.66 Hz, 81.59 Hz, and 123.76 Hz, respectively, demonstrating effective electronic frequency tunability of the proposed filter configuration.

Table 2. Simulated various filtering responses of the proposed voltage mode DDTAs based universal filter.

S. No	Proper Selection of inputs	Outputs	Simulated Filtering Responses
1.	1) $V_{in4} = V_{in5}$, for Inverting 2) $V_{in4} = V_{in5}$, for Non Inverting	V_{o4} V_{o1}	LPF
2.	1) $V_{in1} = V_{in4}$, for Non Inverting 2) V_{in3} for Inverting	V_{o1} V_{o3}	HPF
3.	1) V_{in3} for Non Inverting 2) $V_{in1} = V_{in5}$ for Inverting	V_{o1} V_{o2}	BPF
4.	$V_{in4} = V_{in5}$ for Non Inverting	V_{o3}	BSF/BRF
5.	$-V_{in2} = V_{in4} = V_{in5}$ for Non Inverting	V_{o3}	APF

The simulation results presenting the start of the oscillation and the steady state of the quadrature oscillator have been reported in Figure 8: (a) and (b). The oscillation frequency is 69.86 Hz, and the THD for outputs V_3 and V_4 are 1.18% and 1.31%, respectively.

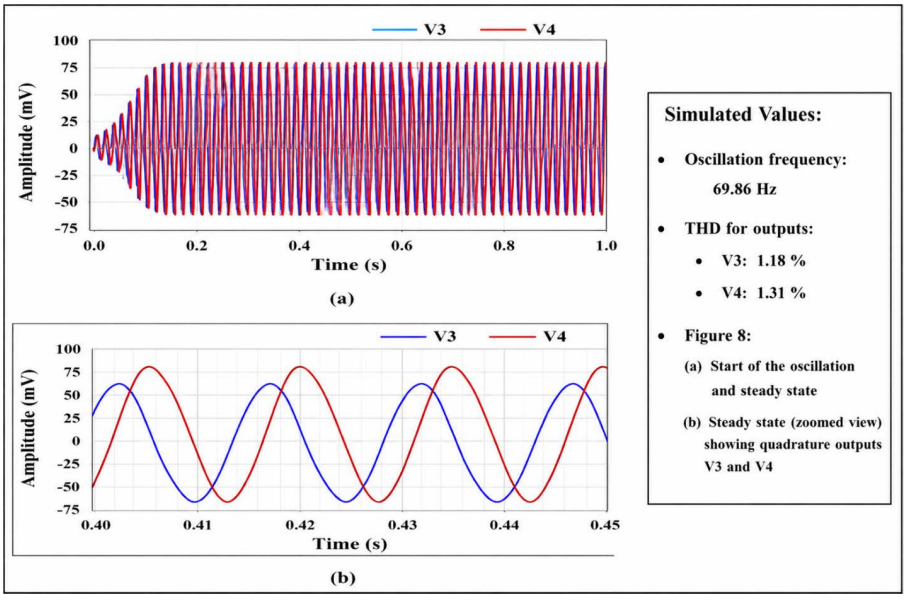

Figure 8. (a) Simulated starting the oscillation and (b) the steady state condition.

Table 3 presents the comparative study with the proposed filter with others in the literature [1] [2] [4] [10]. It is evident that the proposed filter and Quadrature oscillator yield the highest number of filtering functions with lowest power supply 0.20 V and lowest power consumption, thanks to the innovative CMOS structure of the DDTA.

Table 3. Presents the comparative study with the proposed filter with others in the literature.

S. No	Features	Proposed	[1]	[2]	[4]	[10]
1.	No of Active & Passive Components	2 DDTAs, 2 C	2 VGDA, 2C	1 CFOA, 2R, 1C	3CFOA, 5R, 2C	3 IC LT128, 4R, 2C
2.	Realization Technology	CMOS 180 nm	CMOS 0.18 μm	OrCADE PSPICE	CMOS 0.18 μm	PSPICE
3.	Types of Filter	VM MIMO	Mixed Mode	Inverting	Inverting	Multifunction
4.	Offering Universal Oscillator	Quadrature	Dual Mode Quadrature	SIMO Quadrature	Quadrature	No
5.	Power Supply Voltage (V)	0.20 V	±5 V	±15 V	±0.9 V	±5 V
6.	Electronically Tunability	Presents	Presents	No	gain-independent controllability	Presents

6. Conclusions

This work introduces a novel Differential Difference Transconductance Amplifier (DDTA) architecture capable of operating at an ultra-low supply voltage of 0.20 V while providing a rail-to-rail input voltage swing. The applicability of the proposed DDTA is demonstrated through the realization of a universal filter and a quadrature oscillator using only two DDTAs and two grounded capacitors. The performance and practical feasibility of the proposed circuits are validated through both PSPICE simulation results and experimental analysis.

The key features of the proposed configuration are summarized as follows:

1) The circuit requires a reduced number of passive components and does not impose component-matching constraints.

2) Independent and fully uncoupled control of the condition of oscillation (CO) and frequency of oscillation (FO) is achieved.

3) The proposed DDTA structure operates reliably at an extremely low supply voltage of 0.20 V while maintaining rail-to-rail input operation.

4) As practical applications, a universal filter and a quadrature oscillator employing two DDTAs and two grounded capacitors are realized.

5) Theoretical analysis and simulation results consistently confirm the correct functionality and robustness of the proposed circuits.

6) The configuration supports electronic tuning of the pole frequency, with simulation results demonstrating stable operation over a wide range of operating conditions.

7) Owing to its ultra-low voltage operation and low power consumption, the proposed design is highly suitable for integration into compact, power-constrained systems such as biomedical instrumentation and low-frequency, low-voltage sensor applications.

Conflicts of Interest

The author declares no conflict of interest.

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