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Experimental Analysis of Seven-Level Cascaded VSI with SVPWM Algorithm Utilizing FPGA for Photovoltaic System

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Abstract

This paper presents field programmable gate array (FPGA) implementation of space vector pulse width modulation (SVPWM) algorithm for a three-phase seven-level cascaded H-bridge multilevel inverter (CHMLI) for photovoltaic (PV) systems. The maximum power point tracking (MPPT) algorithm is solved by fuzzy logic controller. SVPWM algorithm uses a simple mapping to generate gate signals for the inverter. A digital design of SVPWM generator using hardware description language (VHDL) is proposed and implemented on FPGA. This is done to achieve high dynamic performance with low total harmonic distortion (THD). The results of proposed seven-level cascaded voltage source inverter (VSI) are compared with the five-level inverter in terms of THD. The simulated results are also validated through suitable experiments.

Keywords

Photovoltaic (PV) System, Cascaded H-Bridge Multilevel Inverter (CHMLI), Space Vector Pulse Width Modulation (SVPWM), Field Programmable Gate Array (FPGA), Total Harmonic Distortion (THD)

1. Introduction

In the current scenario, there is a steep rise in the interests in harvesting and utilizing alternative energy sources for furnishing part of the current and future energy rising demand. Some of the energy sources are wind energy and solar energy. In fact, fossil, the conventional energy source, is exhausting. Photovoltaic (PV) is one of the important renewable energy sources, especially for remote locations where utility power is unavailable [1]. The installation of PV generation systems is rapidly growing due to concerns related to environment, global warming, en-

ergy security, technology improvements and decreasing costs [2]. Most of PV-related high-voltage applications require inverters as the interfacing units incorporate dc-dc converters. One of the primary causes of PV system is attributed to the inverter failure due to self-consumption losses [3], generation of electromagnetic interference, and harmonics [4], high-speed and frequency capability for generating pulse width modulation (PWM) and its dead-time effects [5]. Thus, the effectiveness of inverter control system, e.g. controller, control strategy, is the key to the success of PV system applications. Many maximum power point tracking (MPPT) algorithms have been proposed to extract maximum power from the PV array [6].

Multilevel inverters are increasingly being used in high-power medium voltage applications due to their superior performance compared to two-level inverters, such as lower common-mode voltage, lower dv/dt, lower harmonics in output voltage and current and also reduced voltage on the power switches. Different types of multilevel inverter topologies are presented in [7]. Many methods of PWM techniques are used to control the inverter [8]. A novel simplified multilevel space vector modulation scheme based on two-level inverter is proposed [9]. A new multilevel inverter topology that produces three dodecagonal voltage space vectors is presented [10].

Various types of controllers employed in inverters are discussed in [11]. The FPGA is a sub-class of application-specific integrated circuit which provides characteristics such as fast prototyping and higher switching frequency [12]. The three-phase cascaded multilevel inverter with digital controller for reducing power quality issues for solar energy applications is explained [13]. The modelling and simulation of three-phase five-level diode clamped multilevel inverter (DCMLI) using sinusoidal PWM for grid connected photovoltaic system with fuzzy MPPT is presented [14]. FPGA based SVPWM five-level cascaded H-bridge multilevel inverter (CHMLI) with perturbation and observation (P & O) MPPT and SVPWM five-level DCMLI with fuzzy logic control (FLC) MPPT for photovoltaic system are proposed in [15] [16]. The THD minimization of the output voltage of multilevel inverters and the investigation of extension of quasi-two-operation concept of DCMLI to three-level operation [17] [18] are explained. According to the standard Std IEEE-929-2000 [19], a lower percentage of total harmonic distortion (THD) indicates higher quality of an output waveform for utility interface of PV systems.

In this paper, seven-level CHMLI is proposed which is utilizing FPGA for SVPWM technique. The proposed system is shown in **Figure 1(a)**. In this system, a PV cell is represented by a current source in parallel with diode and a series resistance as shown in **Figure 1(b)**. The seven-level CHMLI model and control algorithm are developed and simulated in the SimPowerSystem block set environment. Indeed, the paper proposes a system consisting of a PV array connected to the three-phase multilevel CHMLI which is connected to the three-phase load. The two types of control structure are used in this paper as follows. 1) MPPT control and 2) inverter control.

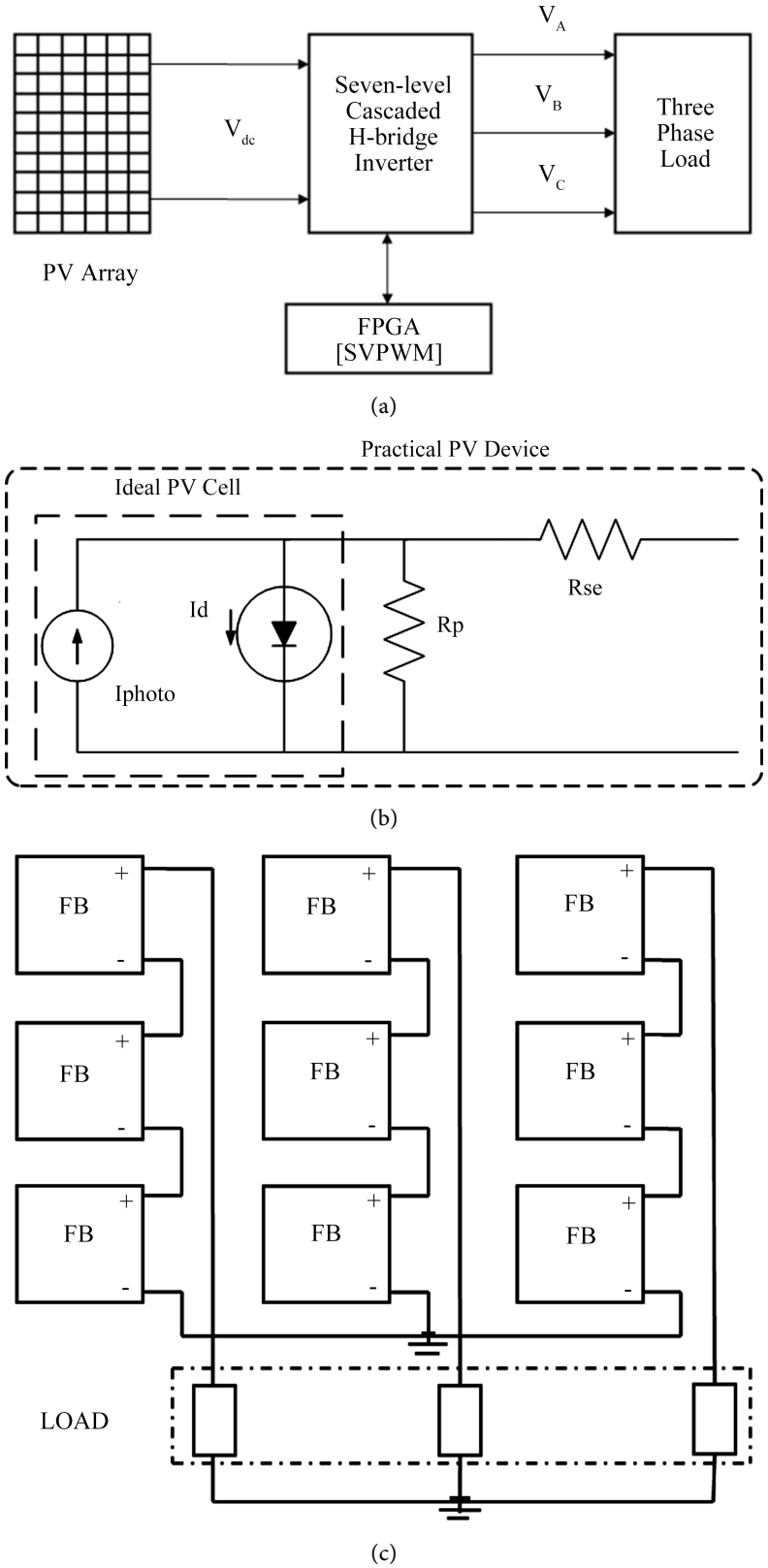


Figure 1. Proposed PV connected CHMLI. (a) General diagram of three phase load connected photovoltaic system; (b) Equivalent circuit of a PV cell physical model; (c) Three-phase seven-level CHMLI circuit diagram.

The main property of the MPPT control is to extract the maximum power from the PV generator and improve energy conversion efficiency under different environmental conditions. Inverter control is used to convert DC input to AC output at the same waveforms as the three-phase lines and to ensure high quality of the output power. In this proposed scheme, the ON-time calculation is simple due to the use of two-level SVPWM. The ON-time calculation equations do not change with the position of the reference vector. Any switching sequence can be executed with respect to triangle Δj, leading to a simplicity and flexibility of optimizing the inverter switching sequence.

2. Seven-Level Cascaded H-Bridge Inverter Topology

A cascaded multilevel inverter consists of a series of H-bridge (single-phase, full-bridge (FB)) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. A three-phase seven-level cascaded H-bridge circuit diagram is shown in **Figure 1(c)**. Each SDCS is connected to H-bridge inverter. The ac terminal voltages of different level inverters are connected in series.

An n-level cascaded H-bridge inverter typically consists of $2(n-1)$ main switching devices, $2(n-1)$ main diodes and $(n-1)/2$ capacitors on the DC bus. Unlike the diode-clamp inverter, the cascaded inverter does not require any voltage-clamping diodes. The phase output voltage is synthesized by the sum of six inverter output voltages Van = Va1 + Va2 + Va3 + Va4 + Va5 + Va6. Each inverter level can generate three different voltage outputs, +Vdc, 0 and −Vdc by connecting the dc source to the ac output side by different combinations of the four switches, Sp1, Sp2, Sn1 and Sn2. When the switches Sp1 and Sp2 are turned ON, it gives Va6 = +Vdc. When the switches Sn2 and Sn1, turned ON, it gives Va6 = −Vdc. When the all switches are turned OFF, it gives Va6 = 0. The ac output of each of the different level full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. If NS is the number of dc sources, the output phase voltage level is $n = 2NS + 1$.

Controlling the conduction angles at different inverter levels can minimize the harmonic distortion of the output voltage. If the phase current ia, is sinusoidal and leads or lags the phase voltage Van by 90˚, the average charge to each dc capacitor is equal to zero over one cycle. Therefore, all SDCS capacitor voltages can be balanced. Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase-leg-switching timings. Switches Spx and Snx (x = 1, 2, 3, 4, 5, 6) are arranged in pairs and operate in a complementary mode where Spx as positive switches and Snx as negative switches. State condition "1" means the switch is ON and "0" means the switch is OFF.

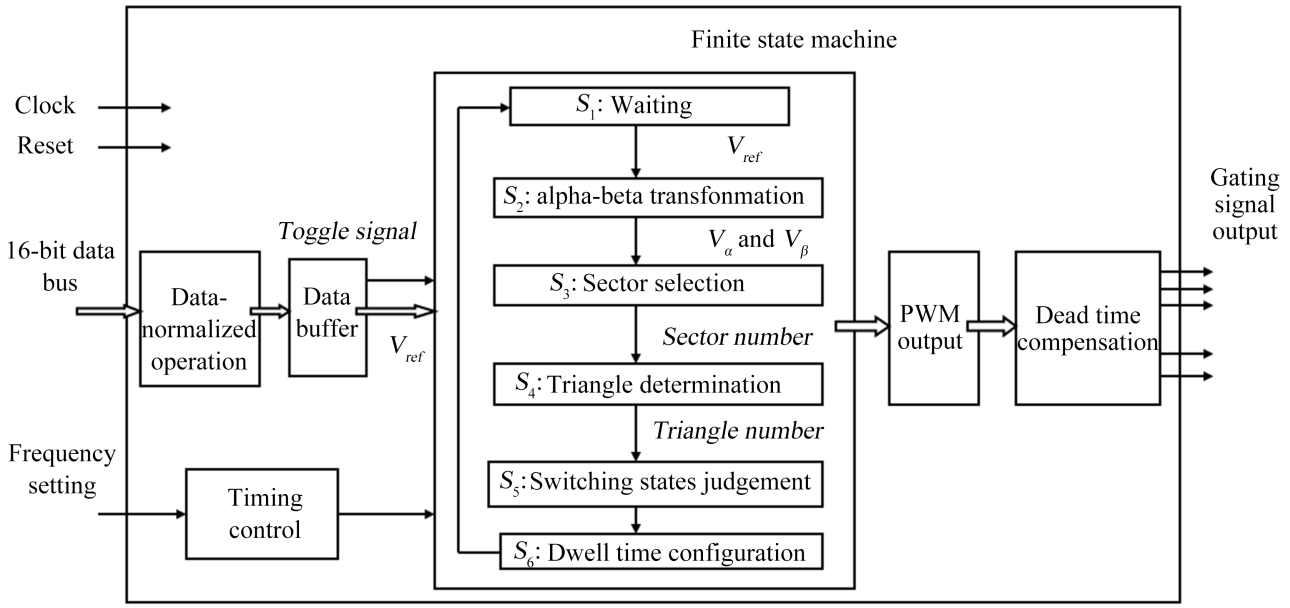
3. PV Inverter Controller

3.1. FPGA Based Controller

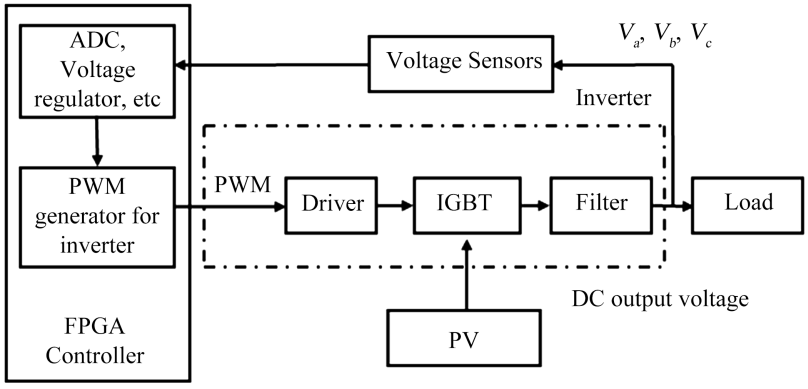
A FPGA is a silicon chip containing an array of configurable logic blocks, digital

clock manager, hardware multipliers and memory. The FPGA used in this project is Xilinx Spartan 3A, which has 1.8 Million gates. An ASIC can perform a single function for the lifetime of the chip whereas FPGA can be reconfigured to perform different function in a matter of microseconds. The design used Xilinx development tool and is realized in a single FPGA chip with no external memory. The whole system is implemented in only a single chip with more reliable, faster design, less verification time, and high performance. A standard FPGA design flow should include circuit design and entry, functional simulation, synthesize, post synthesize simulation, place-and-route, post place-and-route simulation, board level simulation and download.

The block diagram for FPGA implementation of SVM control strategy and hardware logic flow is shown in **Figure 2(a)**. The SVM generator based on finite state machine (FSM) is to implement the SVM algorithm. The FSM consists of six states, which are waiting, α-β transformation, sector selection, triangle determination, switch states judgment, and dwell time configuration.



(a)



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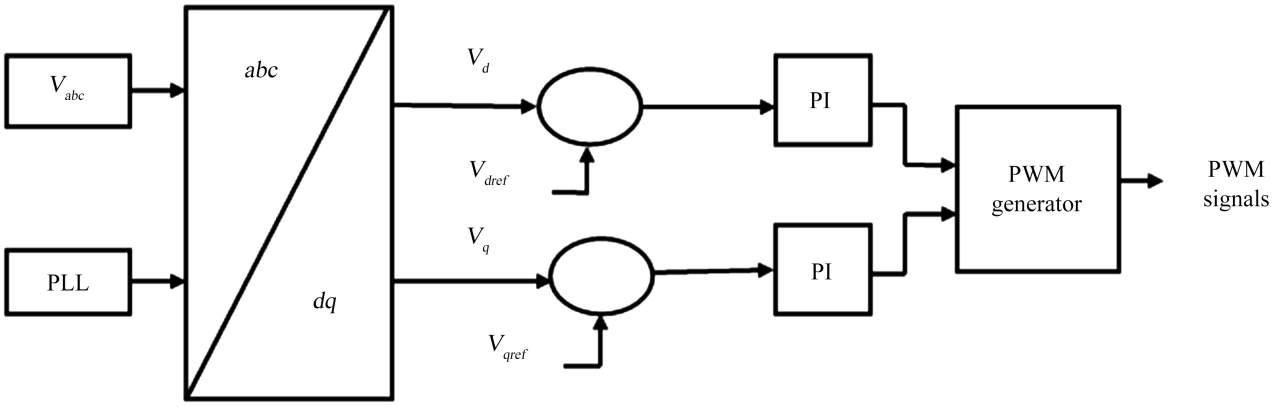

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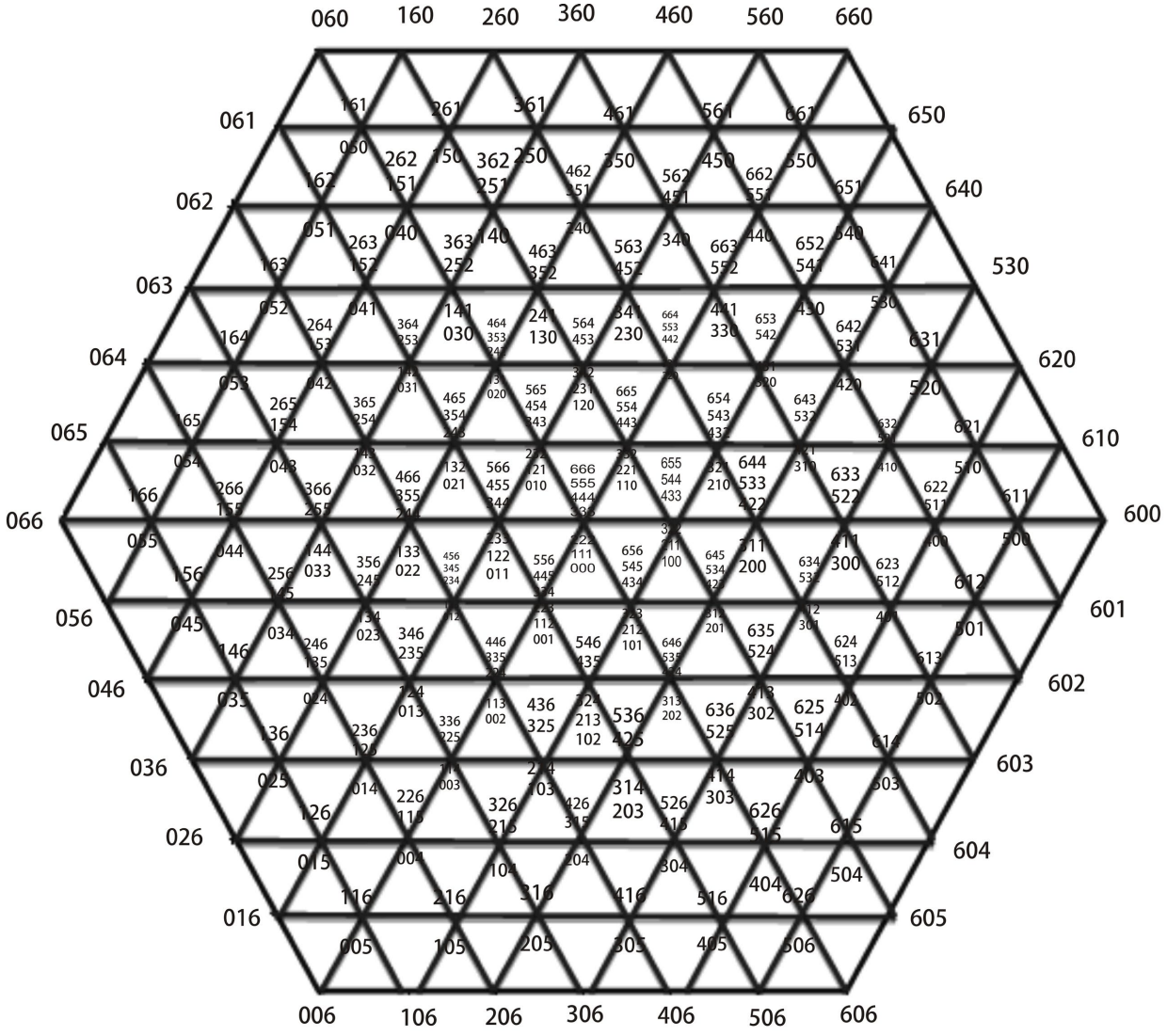


(d)

Figure 2. Control scheme implemented in FPGA based controller. (a) Block diagram for FPGA implementation SVM control with finite state machine; (b) Block diagram of FPGA-controlled inverter; (c) Block diagram of the voltage control scheme; (d) Space vector diagram for seven-level inverter.

In this paper, VHDL coding is used to generate the SVPWM for the inverter circuit. Simulation steps are as follows.

1) Initialize system parameters using FPGA

2) VHDL coding are used to: a) Determine sector, b) Determine time duration T_a, T_b, T_0 and c) Determine the switching time of each sector

3) Generate the inverter output voltage

4) View the SVPWM waveforms through Xilinx.

FPGA resource utilization (number of logic gates/blocks used), clock cycles, and execution time of the VHDL code compared to traditional DSP or microcontroller implementations based on [15] [16].

3.2. Control Strategy

The digital PI controller can be employed to regulate the three-phase PV CHMLI ac output voltage. **Figure 2(b)** describes the block diagram of a FPGA controlled inverter implemented in this work.

The system consists of FPGA based controller, PV array, inverter, three-phase load and voltage sensors. As part of the voltage regulation feedback loop, three voltage sensors are used for interfacing the inverter output voltages V_a, V_b and V_c, with the FPGA based controller. With the specific voltage gains, these sensors attenuate the voltage to adapt to the FPGA working voltages. The inverter output voltages V_a, V_b and V_c, with unity power factor are assumed as in (1) - (3).

$$V_a = V \sin \omega t \tag{1}$$

$$V_b = V \sin\left(\omega t - \frac{2\pi}{3}\right) \tag{2}$$

$$V_c = V \sin\left(\omega t + \frac{2\pi}{3}\right) \tag{3}$$

where V is the voltage magnitude and ω is the output frequency. The sensors scale down these voltages and feed them to the analog-to-digital converter (ADC) channels of the FPGA based controller for further signal processing. These signals are sampled and fed to the voltage regulator block for voltage regulation. For standalone inverter, the strategy is to regulate the output voltage supplied to the load. This issue is addressed by the control strategy presented in **Figure 2(c)**.

Utilizing the park's transformation method, the sampled signals are transformed from the abc stationary frame into synchronous rotating frame, dq (direct-quadrature). Consequently, the two components, V_d and V_q are regulated based on their respective references which are V_{dref} and V_{qref} respectively. In this transformation which assumes the balanced loads condition, the 50 Hz synchronization signal is employed derived from the phase-locked loop (PLL) block. With this transformation, the PI controllers are able to operate effectively on the two components, reducing the steady-state errors, thus, regulates the output voltage. Moreover, the power with unity power factor is generated and transferred. The PI controller algorithm in time domain is described in (4).

$$u(t) = K_P e(t) + K_i e(t)\,dt \tag{4}$$

where $u(t)$ is the output of the PI controller, K_P and K_i are the gains of the proportional and integral terms, and $e(t)$ is the error voltage which is the difference between the reference voltage and the measured one ($V_{dref} - V_d$). The output voltage as in (1) - (3) is sampled based on the sampling time. In every sampling time, the PI controller generates the output voltage, in such a way that the error signal is kept to a minimum value. Thus, the system is capable of keeping the output voltage as close as possible to the reference voltage. As a result the inverter output voltage can be controlled and stabilized. This voltage regulation is made possible by the accomplishment of the PWM technique. To obtain a sinusoidal shape ac output waveform, a SVPWM switching technique is implemented in the inverter control algorithm.

3.3. SVPWM Algorithm of ON-Time Calculation for a Multilevel Inverter

In this paper, SVPWM technique is used to generate PWM control signals to the inverter. Modulation index (MI) is defined as in Equation (5)

$$MI = \frac{V_{P1}}{V_{P1SIX}} \tag{5}$$

In Equation (5), V_{P1} is the peak value of fundamental voltage and V_{P1SIX} is the peak value of fundamental voltage at six step operation. For a n-level cascaded topology $V_{P1SIX} = (2/\pi)(n-1)V_{dc}$, where V_{dc} is the dc link voltage. For a diode clamped topology $V_{P1SIX} = (2/\pi)(V_{dc})$, this is same as two-level inverter. The SVM is used to compensate the required volt-seconds using discrete switching states and their ON-times produced by inverter.

In a two level inverter, ON-time calculation is based on the location of reference vector within a sector S_i, $i = 1, 2, \ldots, 6$. For a two-level inverter, volt-second equation is,

$$V^z T_S = V_X T_a + V_Y T_b \tag{6}$$

The volt-seconds in terms of components V^z, V_X and V_Y of along α-β axis are,

$$V_\alpha^z T_S = T_a + 0.5T_b \tag{7}$$

$$V_\beta^z T_S = hT_b \tag{8}$$

$$T_S = T_a + T_b + T_0 \tag{9}$$

Solving Equations (7)-(9), obtain for the calculation of ON-times,

$$T_a = T_S\left[V_\alpha^z - \frac{V_\beta^z T_S}{2h}\right] \tag{10}$$

$$T_b = T_S\left[\frac{V_\beta^z}{h}\right] \tag{11}$$

$$T_0 = T_S - T_a - T_b \tag{12}$$

In Equations (10)-(12), h is height of the triangle of sector S_i {h = 0.866 or $\sqrt{3}/2$ }, assuming that the sides of the equilateral triangle are unity. $T_S = 1/(2f_S)$, fS is the switching frequency. **Figure 2(d)** shows the space vector diagram for seven-level inverter.

Each sector can be split into $(n-1)$ triangles, where n indicates level of the inverter. For any given reference vector, the sector of operation and its angle within the sector is determined by using Equation (13) and Equation (14), respectively.

$$S_i = \text{int}\left(\frac{\theta}{60}\right)+1 \tag{13}$$

$$\gamma = \text{rem}\left(\frac{\theta}{60}\right) \tag{14}$$

where, $\theta\,(0^\circ \le \theta \le 360^\circ)$ is the angle of the reference vector with respect to α axis, $\gamma\,(0^\circ \le \gamma \le 60^\circ)$ is the angle within the sector and $S_i\,(1 \le S_i \le 6)$ is its sector operation, int and rem is standard math function of integer and reminder. The space vector diagram of a three-phase VSI is an hexagon, consisting of six sectors. SVPWM algorithm is to identify the triangle in which the tip of the reference vector is located. Each triangle can be treated as a vector of a two-level inverter. The ON-time can be calculated using small vector analogy ON-time equation of the two-level inverter. In each sector, triangle can be classified into two types. Type-1 triangle has its base side at the bottom. Type-2 triangle has its base side at the top. The triangle number Δ_j can be determined in terms of two integer variables I_1 and I_2, which are dependent on the position of reference vector (V_α, V_β).

$$I_1 = \text{int}\left(V_\alpha + \frac{V_\beta}{\sqrt{3}}\right) \tag{15}$$

$$I_2 = \text{int}\left(\frac{V_\beta}{h}\right) \tag{16}$$

The Equation (15) signifies part of the sector between the lines $y+\sqrt{3} = \sqrt{3}I_1$ and $y+\sqrt{3}x = \sqrt{3}\left(I_1+1\right)$. This forms one region and the Equation (16) signifies part of the sector between the lines $y = h\cdot I_1$ and $y = h\cdot\left(I_1+1\right)$. This forms another region. The tip of reference vector is situated at the intersection of these two regions inclined at 120˚ and forms triangle or rhombus.

This rhombus is made of two triangles. Let ($V_{\alpha S}$, $V_{\beta S}$) are the co-ordinates of the reference vector with respect to the origin of the rhombus.

$$V_{\alpha S} = V_\alpha - I_1 + 0.5I_2 \tag{17}$$

$$V_{\beta S} = V_\beta - I_2 h \tag{18}$$

In Equation (17) and Equation (18), ($V_{\alpha S}$/ $V_{\beta S}$) is the slope of the line between the origin of the rhombus and the reference vector and it is compared with slope of the diagonal of the rhombus which is $\sqrt{3}$. The slope comparison is done by evaluating inequality ($V_{\beta S} \le \sqrt{3}V_{\alpha S}$) and to determine the small vector VZ and the exact triangle number Δ_j. If the ($V_{\beta S} \le \sqrt{3}V_{\alpha S}$), which indicates triangle of type-1

and these triangles are similar to sector-1 of two-level inverter. The triangle number Δ_j is obtained as

$$\Delta_j = I_1^2 + 2I_2 \tag{19}$$

If ($V_{\beta S} > \sqrt{3}V_{\alpha S}$), which indicates the triangle of type-2 and these triangles are similar to sector 2 of two-level. The triangle number Δ_j is obtained as

$$\Delta_j = I_1^2 + 2I_2 + 1 \tag{20}$$

where, Δ indicates the triangle and j is the triangle number and hence Δ_j is an integer and signifies jth triangle in the sector. Using Equation (19) and Equation (20), to identify triangle in a sector and the on times are calculated using Equation (10) to Equation (12). The Δ_j is formulated to provide a simple way of arranging the triangle, leading to ease of identification and extension to any level and it greatly simplifies the PWM process as switching state can be easily mapped with respect to Δ_j.

3.4. SVPWM Algorithm of Reducing Switching Loss

In seven-level inverter, the redundant switching states cause certain voltage vectors correspond to 2/3/4/5/6/7 switching states. This algorithm is used to reduce the switching times and switching loss of power devices. The main principle of the algorithm is that, the changing of switch states causes only the voltage (switch state) of the one phase change every time. In seven-level vector diagram, when the rotating vector rotates from sector S186 to sector S187 the switching states will modulate as following switching sequence (661 → 660 → 650 → 550 → 550 → 650 → 660 → 661) → (661 → 660 → 560 → 550 → 550 → 560 → 660 → 661). When the rotating space vector VZ is in sector S186, VZ can be synthesized by space vector (expressed by switching state) (661 or 550), (650), and (660). When VZ falls in to sector S187, space vectors (661 or 550), (660), and (560) are selected to synthesize VZ. The switching states 661 and 550 express the same voltage vector and it is used as the starting state and ending state to complete the modulation process. There are a certain number of transitional switching states, but this will not change the overall output voltage magnitude and the duration of each output voltage vector.

3.5. Inverter Control Algorithm

The inverter control is based on a decoupled control of the active and reactive power. The DC voltage is set by a PI controller that compares the actual DC bus voltage and the reference generated by the MPPT, and provides i^*d active current reference in a synchronous frame attached at load voltage vector. The other component of current vector Qref represents the reactive current and it can be fixed at zero to maintain almost unity power factor. By applying the inverse park transformation to dq vector components, the desired references Vref are obtained. These are passed to inverter control which gives outputs of pulses to drive the multilevel inverter switches.

As there is no DC-DC converter between the PV generator and the inverter, the PV array configuration has to be chosen so that the output voltage of the PV generator suits the inverters requirements. The lowest DC voltage will occur with high ambient temperature and high irradiance due to the high irradiance, the cell temperature increases which affects the increase in optimal voltage of the PV array. This algorithm has a better rejection of load harmonics, notches, and any other kind of disturbances.

4. Simulation Model

Simulations are performed by using MATLAB/simulink for the proposed system. The PV array used in the proposed system is KC200GT and it is simulated using a model based on [15]. In this PV array, mathematical model can be expressed in Equation (21).

$$I = I_{Photo} - I_{RSat}\left\{\exp\left[\frac{q}{A_D K_B T}\left(V + IR_{Se}\right)\right] - 1\right\} - \frac{V + R_{Se}I}{R_P} \tag{21}$$

where

I_{Photo}—photo current, I_{RSat}—reverse saturation current,

q—electronic charge ($1.60217646 \times 10^{-19}$ C), R_{Se}—series resistance,

R_P—parallel resistance, A_D—dimensionless factor,

K_B—Boltzmann constant (1.38×10^{-23} J/K) and T—temperature.

$$I_{Photo}\left(G_{ira}\right) = I_{SC}\left(\frac{G_{ira}}{G_{iraS}}\right) \tag{22}$$

where

I_{SC}—short circuit current depends linearly on cell temperature,

G_{iras}—standard irradiation (1000 W/m^2).

$$I_{SC}\left(T\right) = I_{SCSat}\left[1 + \Delta I_{SC}\left(T - T_{St}\right)\right] \tag{23}$$

where

ΔI_{SC}—temperature coefficient

T_{St}—standard temperature (298˚K).

I_{Photo} and I_{RSat} depend on the cell temperature and solar irradiation and these can be mathematically expressed as

$$I_{Photo}\left(G_{ira}, T\right) = I_{SCSat}\left(\frac{G_{ira}}{G_{iraS}}\right)\left[1 + \Delta I_{SC}\left(T - T_{St}\right)\right] \tag{24}$$

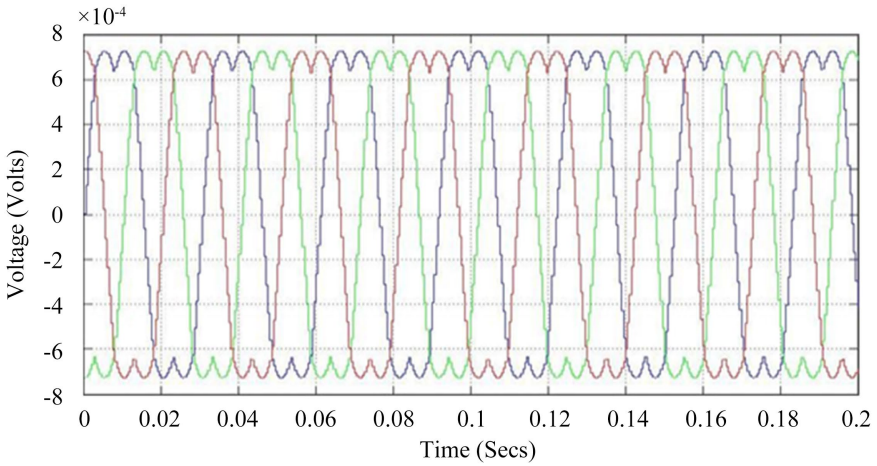
$$I_{RSat}\left(G_{ira}, T\right) = \frac{I_{Photo}\left(G_{ira}, T\right)}{e^{\frac{V_{OC}}{V_t}} - 1} \tag{25}$$

where, V_t is thermal voltage.

An intelligent control technique using FLC is associated to an MPPT control of the PV system, whose main property is to extract the maximum power from the PV generator and improve energy conversion efficiency under different environmental conditions. Internal design, fuzzification process, membership functions,

rule base and defuzzification method used based on [14] [16]. It can deal with imprecise inputs, does not need an accurate mathematical model and can handle non-linearity based on [14] [16]. The SVPWM switching strategy is used in this paper. The SVPWM output is generated from this simulink module. The simulation was carried out for 0.2 seconds and this involves determining the position of reference vector according to fundamental frequency f = 50 Hz, sampling frequency f_s = 10 kHz and time.

According to sector wherein the reference vector is, determine the switching sequence and to calculate the time for different switching states. The switching instant of a SVPWM pulse waveform is shown in **Figure 3(a)**. The modulation index determines the shape of the output voltage of the inverter. FLC controlled MPPT tracks the operating point quickly and accurately with and without change irradiance level. The simulation result of FLC MPPT tracking is shown in **Figure 3(b)**. An irradiance step-change response graph based on [14] provided to substantiate the claim that the MPPT dynamically tracks varying environmental conditions. The decoupling of the voltage loops V^*d and V^*q is good, since the V^*q remains constant under variations which shows high dynamic performance of the controllers.



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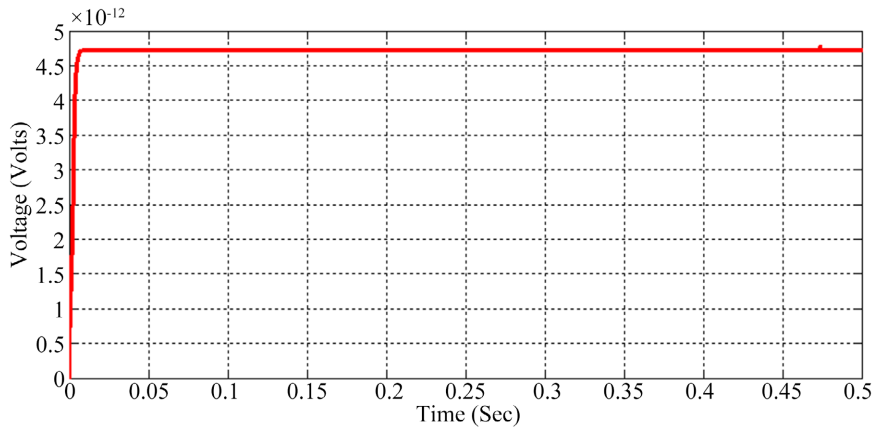

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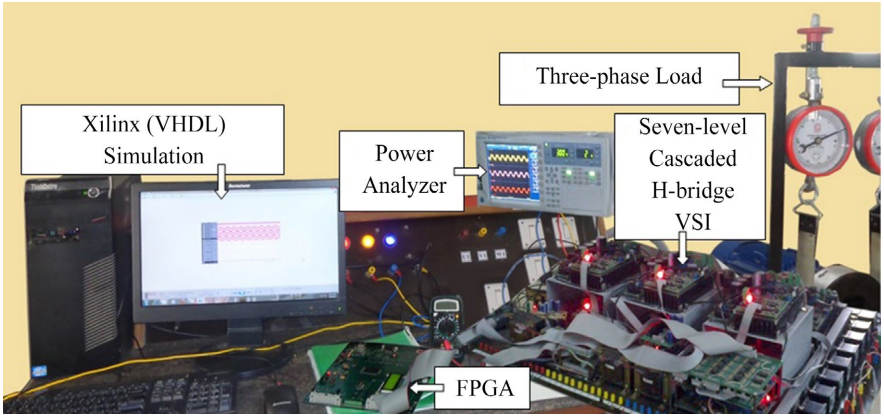


(c)

Figure 3. Proposed SVPWM for PV connected CHMLI. (a) Switching instant of a SVPWM pulse waveform; (b) Fuzzy MPPT control; (c) Photograph of experimental setup.

The performance of the FLC with PV CHMLI also shows that output of the PV follows its reference. The overall operation is governed by the control system where the controller samples the voltages of the inverter and then generates the PWM signals for driving the IGBTs. With the control scheme implementation, the inverter is able to maintain constant phase and line output voltage.

5. Experimental Set-Up

For verification of the simulated model, three-phase seven-level CHMLI prototype was build, tested and evaluated in laboratory which is shown in **Figure 3(c)**. The solar panel is not shown in photograph. The equipment used in the experimental set-up are Xilinx development tool with VHDL coding, FPGA Spartan 3A controller, power analyzer, digital multimeter, IGBT's, IGBT driver are used in PV tied three-phase seven-level CHMLI.

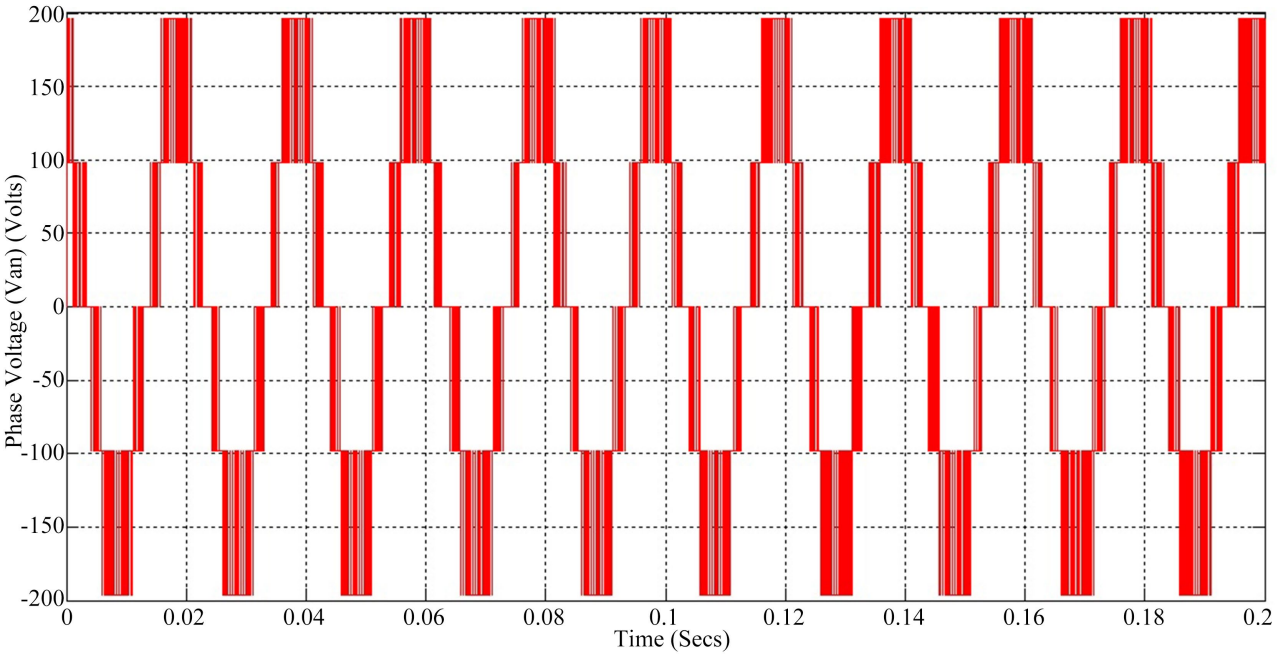
6. Result and Discussion

6.1. Simulation Results

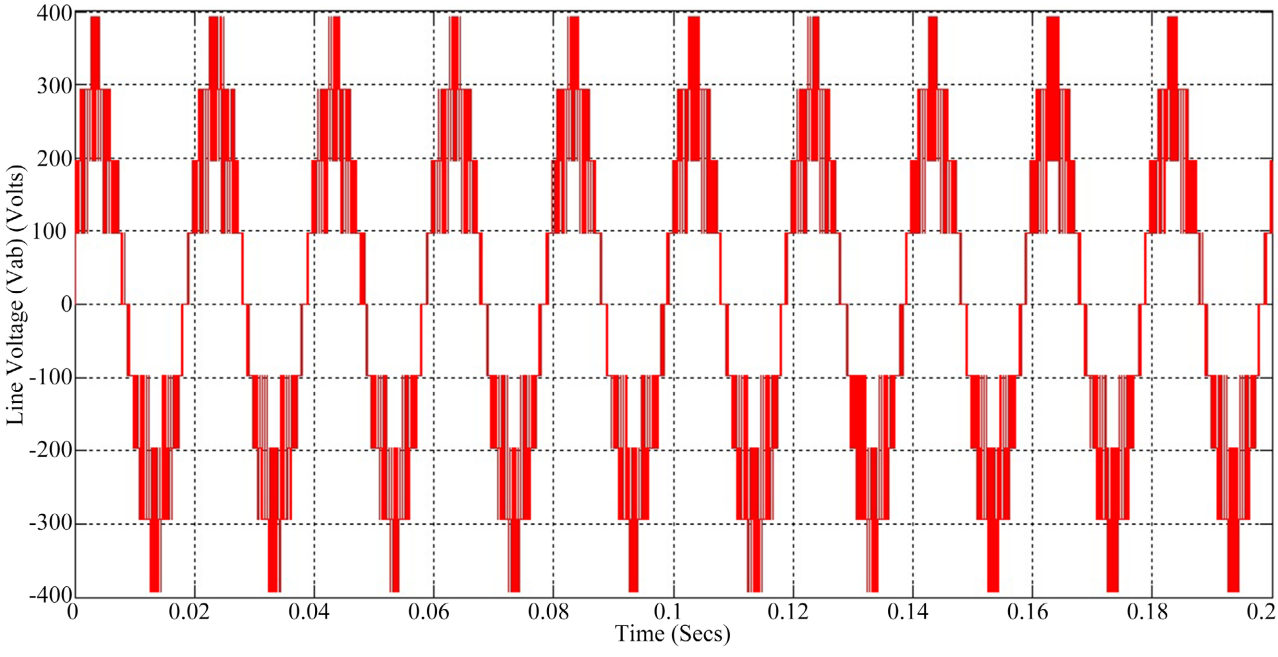
The simulation result of the PV three-phase five-level CHMLI is shown in **Figures 4(a)-(e)**. In the proposed system, FLC controlled MPPT tracks the operating point quickly and accurately with and without change irradiance level.

The decoupling of the voltage loops Vd^* and Vq^* is good, since the Vq^* remains constant which shows high dynamic performance of the controllers. The performance of the FLC with the three-phase five-level and seven-level CHMLI also shows the output of PV follows its reference and there are no effects for the load variation. The simulation result of the output phase voltage and line-to-line voltage of the PV three-phase five-level CHMLI is shown in **Figure 4(a)** and **Figure 4(b)**. This shows that the generated voltage is much improved with the level of inverter. **Figure 4(c)** shows the line voltage waveform THD of the simulated five-level inverter which is 0.80%. It can be seen that the output voltage waveforms are

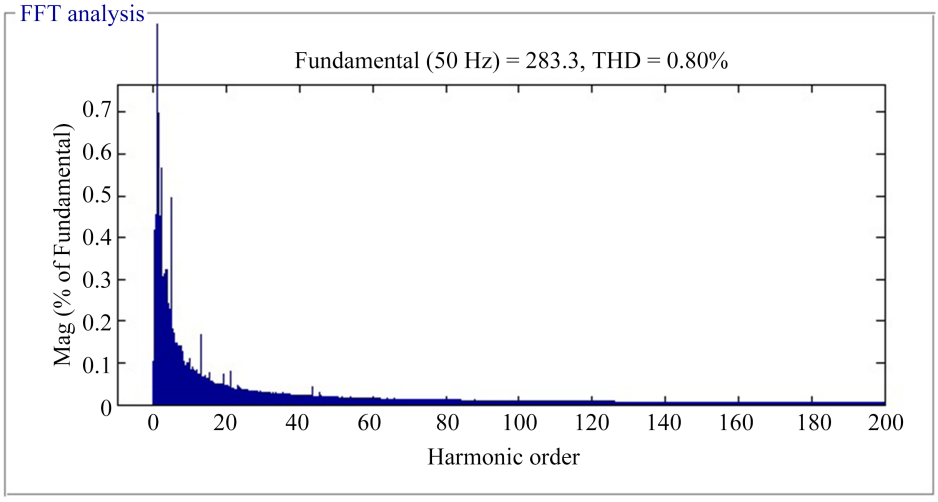
50 Hz sinusoidal, balanced, and displaced to each other by 120˚. It reveals a considerably good transient and steady-state performance of the inverter. The controller manages to precisely track the voltage reference, quickly achieve the steady-state values, and discriminates oscillation around the operating point. These results demonstrate the efficacy of the control strategy and algorithm employing the PI controller. In this scheme, having 10 kHz for the switching frequency, these harmonic components are easily filtered out by the smaller size LC low-pass filter.



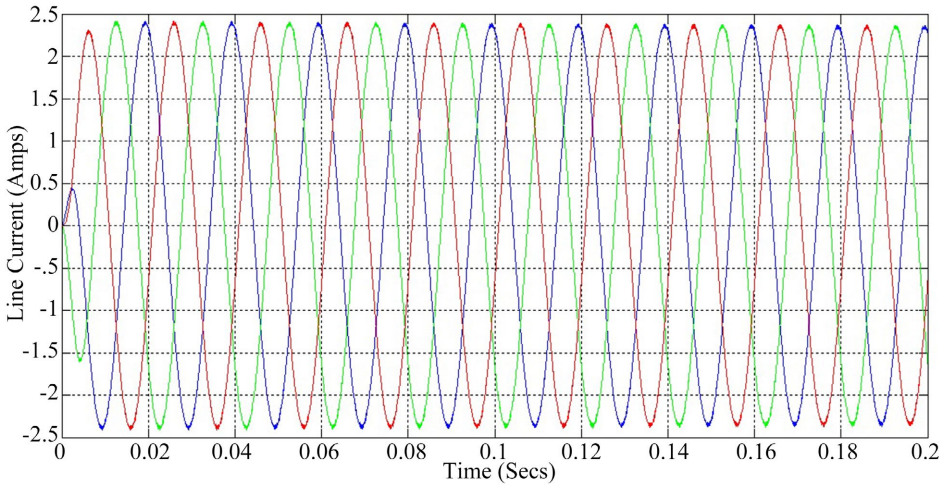
(a)



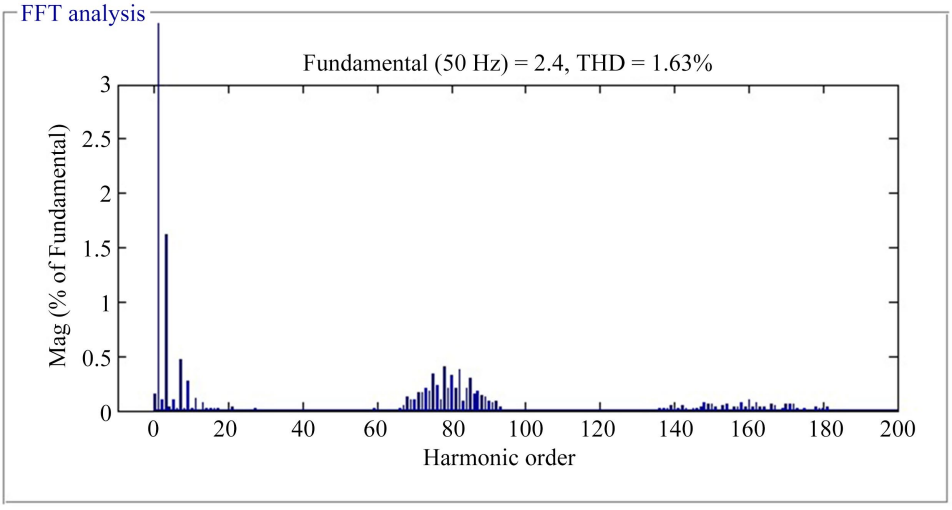
(b)



(c)



(d)



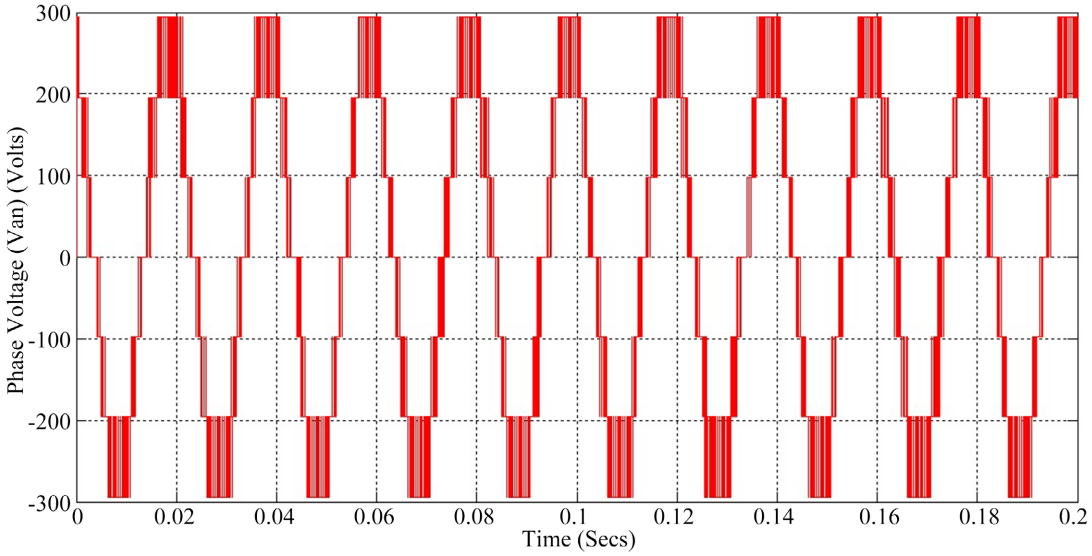
(e)

Figure 4. Simulation result of SVPWM for five-level CHMLI. (a) Phase voltage (Van); (b) Line-to-Line voltage (Vab); (c) Output voltage THD measurement; (d) Three-phase output line current; (e) Output current THD measurement.

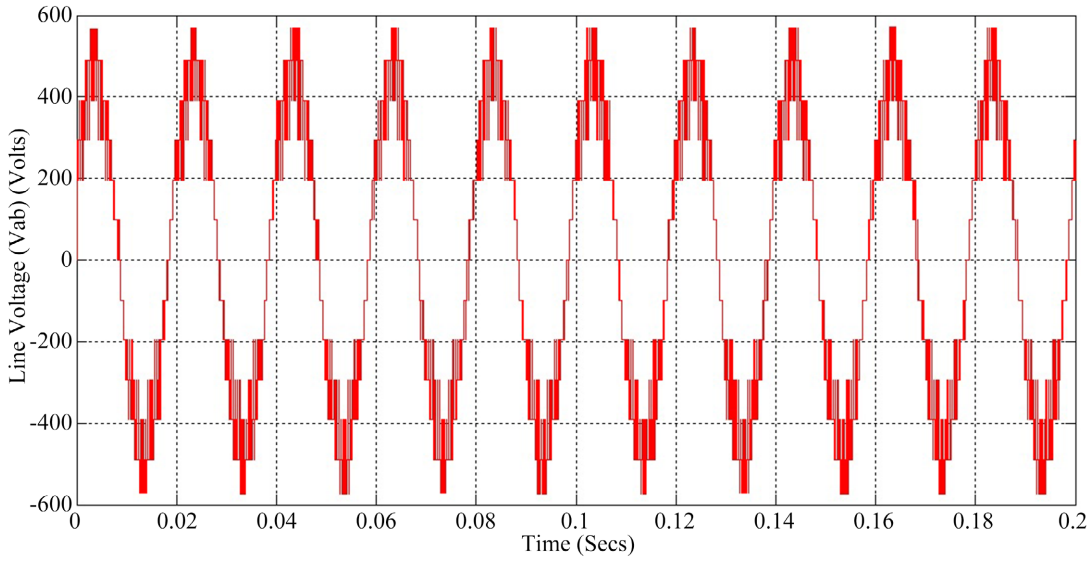
According to the standard Std IEEE-929-2000 [19], the THD of inverters output voltage and current waveforms must be less than 5%. The current waveforms for the three-phase five-level CHMLI are shown in **Figure 4(d)**. **Figure 4(e)** shows the line current waveform THD of the simulated inverter which is five-level for 1.63% and complies with standard. It indicates that most of the harmonics components especially around the 10 kHz (200th harmonic order) switching frequency are filtered out from the inverter output waveforms. They are balanced sinusoidal waveforms of 50 Hz, and 120˚ displacement to each other. Considering the phase relation of both load current and voltage waveform, they reveal in phase relationship, indicating a unity power factor feature which acquires high efficiency. It can be seen that, the most of the harmonics components especially around the 10 kHz switching frequency are filtered out from the inverter output waveforms.

The simulation result of the PV three-phase seven-level CHMLI is shown in **Figures 5(a)-(e)**.

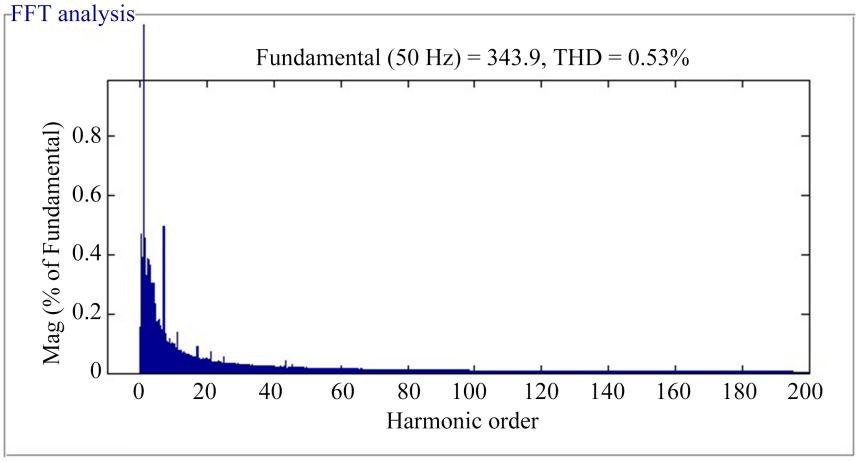
The simulation result of the output phase voltage and line-to-line voltage of the PV three-phase seven-level CHMLI is shown in **Figure 5(a)** and **Figure 5(b)**. This shows that the generated voltage is much improved with the level of inverter. **Figure 5(c)** shows the line voltage waveform THD of the simulated seven-level inverter which is 0.53%. It can be seen that the output voltage waveforms are 50 Hz sinusoidal, balanced, and displaced to each other by 120˚. It reveals a considerably good transient and steady-state performance of the inverter. The controller manages to precisely track the voltage reference, quickly achieve the steady-state values, and discriminates oscillation around the operating point. These results demonstrate the efficacy of the control strategy and algorithm employing the PI controller. In this scheme, having 10 kHz for the switching frequency, these harmonic components are easily filtered out by the smaller size LC low-pass filter. The current waveforms for the three-phase seven-level CHMLI are shown in **Figure 5(d)**. **Figure 5(e)** shows the line current waveform THD of the simulated inverter which is seven-level for 1.08% and complies with standard. It indicates that most of the harmonics components especially around the 10 kHz (200th harmonic order) switching frequency are filtered out from the inverter output waveforms. They are balanced sinusoidal waveforms of 50 Hz, and 120˚ displacement to each other. Considering the phase relation of both load current and voltage waveform, they reveal in phase relationship, indicating a unity power factor feature which acquires high efficiency. It can be seen that, the most of the harmonics components especially around the 10 kHz switching frequency are filtered out from the inverter output waveforms. This proves that the proposed scheme can reduce the THD which is an indispensable condition for PV system. The low THD of both load voltage and load current waveform are mainly contributed by the effectiveness of the components selection of the low pass filter and the SVPWM switching technique implemented in the inverter control algorithm.


Phase Voltage (Van) (Volts)
300
200
100
0
-100
-200
-300
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2
Time (Secs)

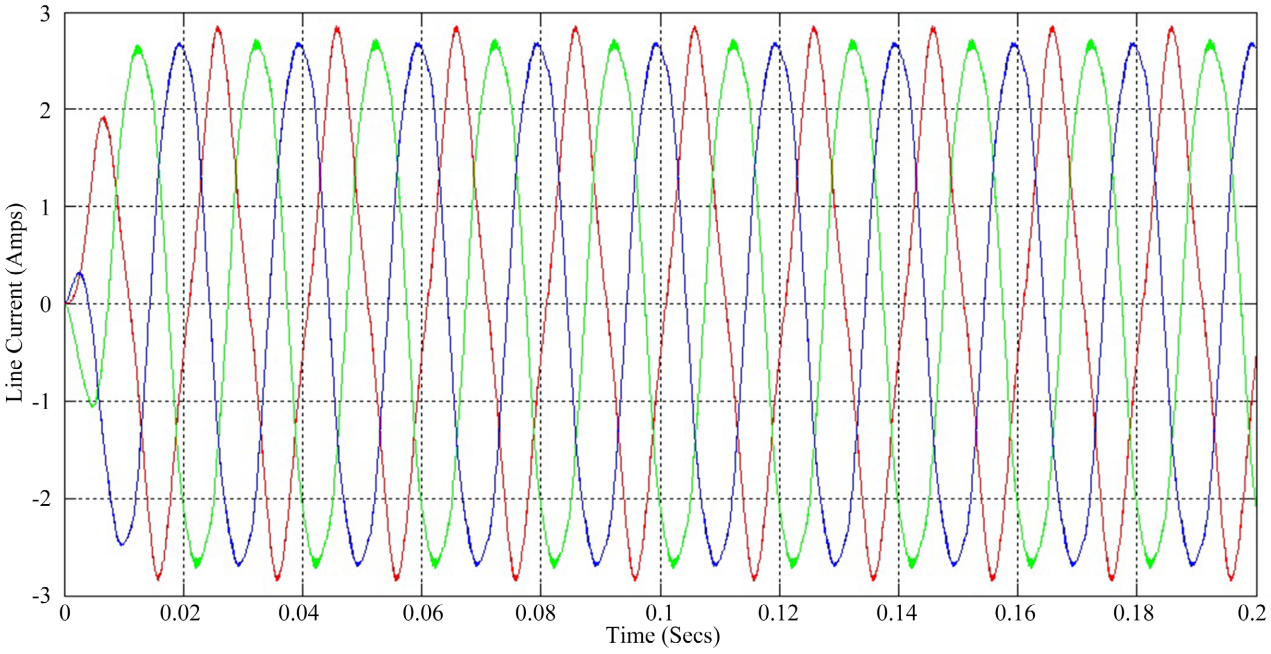
(a)


Line Voltage (Vab) (Volts)
600
400
200
0
-200
-400
-600
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2
Time (Secs)

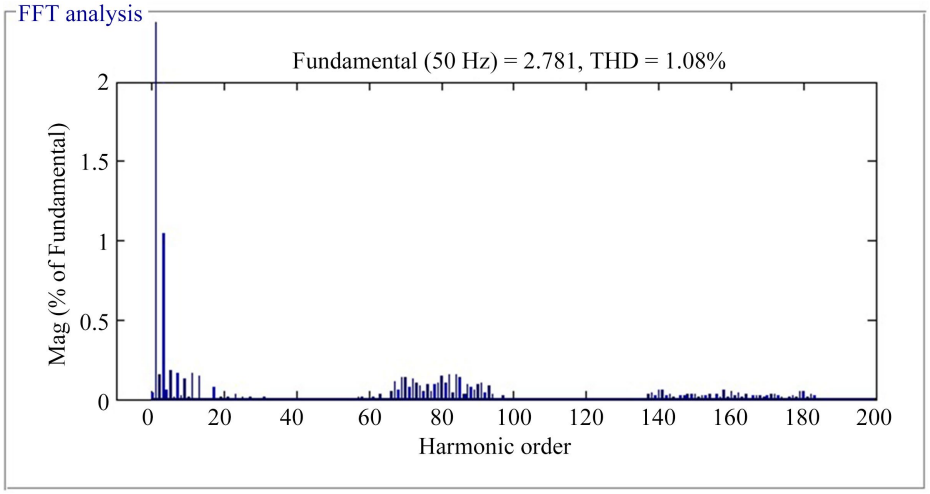
(b)


FFT analysis
Fundamental (50 Hz) = 343.9, THD = 0.53%
Mag (% of Fundamental)
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
180
200
Harmonic order

(c)



(d)



(e)

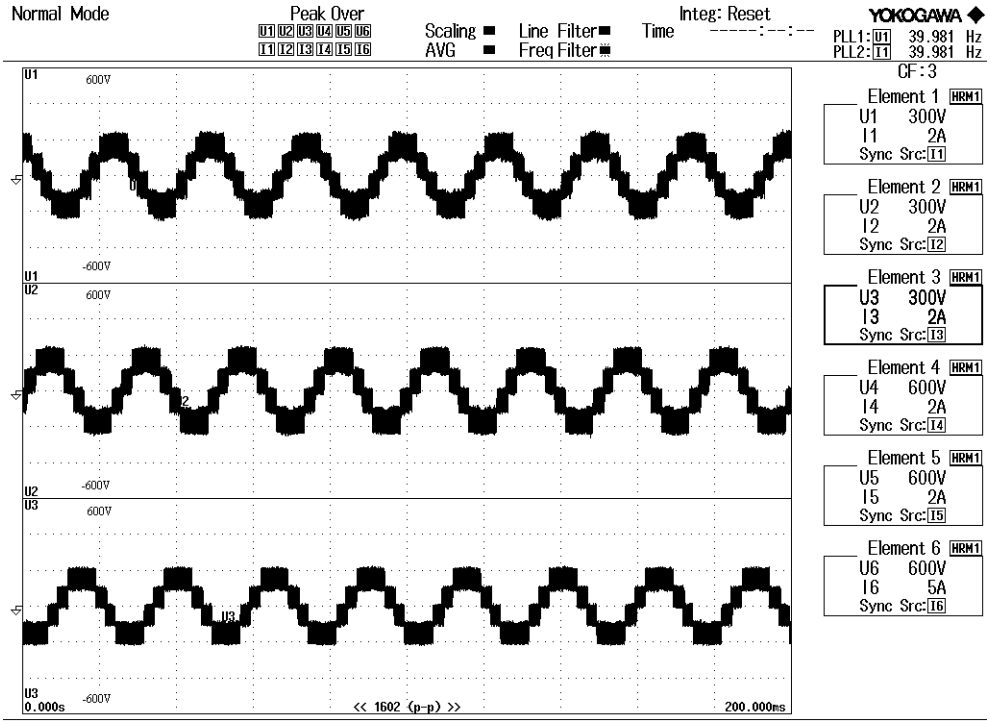
Figure 5. Simulation result of SVPWM for seven-level CHMLI. (a) Phase voltage (Van); (b) Line-to-Line voltage (Vab); (c) Output voltage THD measurement; (d) Three-phase output line current; (e) Output current THD measurement.

6.2. Experimental Results

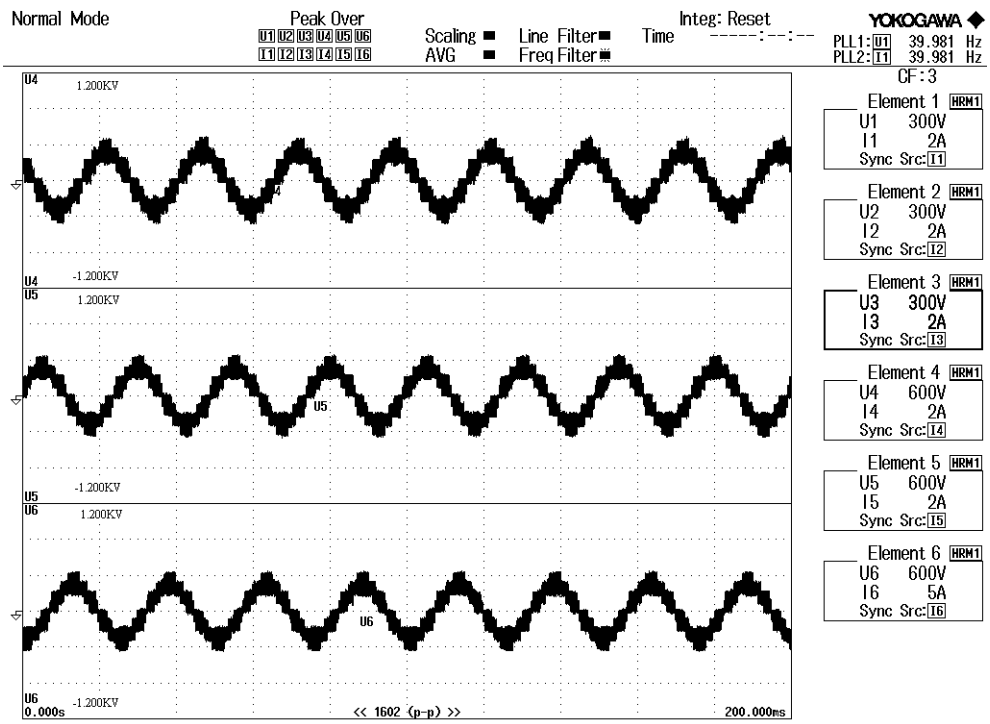
The experimental result of the PV three-phase five-level CHMLI is shown in **Figures 6(a)-(d)**.

The experimental results are presented in order to assess the effectiveness of the proposed three-phase CHMLI model and control algorithm. It also serves as a benchmark which relates the experimental achievements to the simulation and modeling concepts. VHDL code is developed to examine the switching patterns of SVPWM method. This code is synthesized using Xilinx ISE. The FPGA based generalized SVPW modulator is applied to control these PV CHMLI to track the

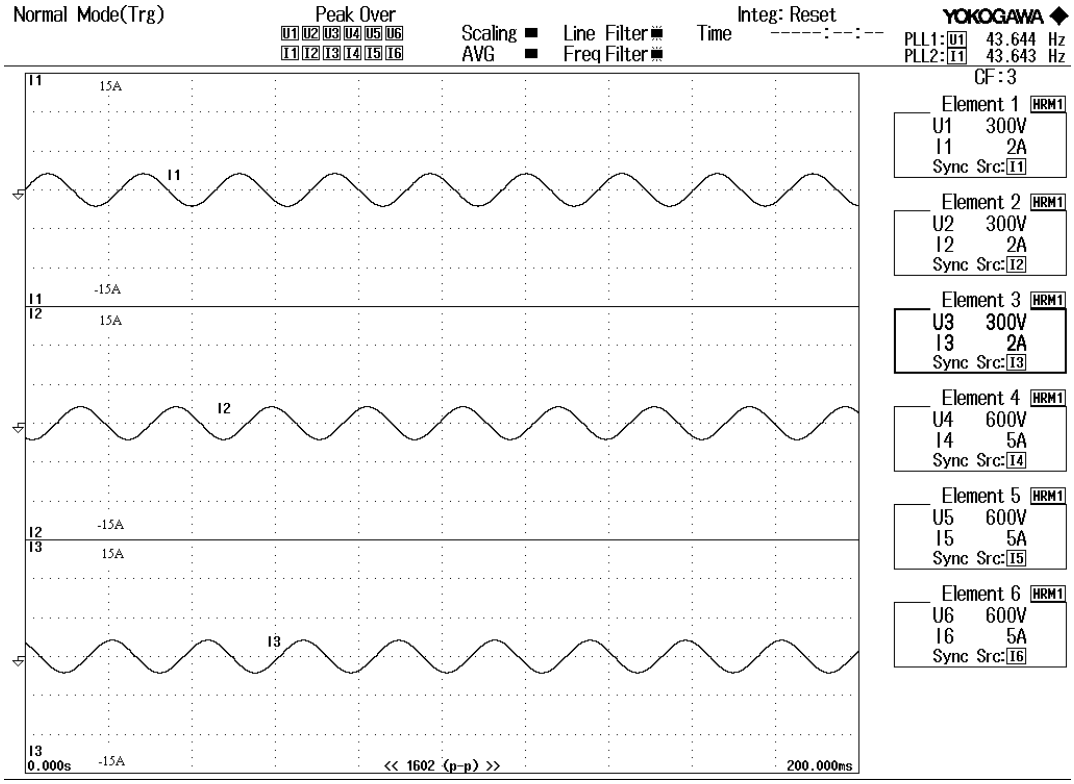
given reference. The output phase voltage and line voltage of the five-level CHMLI is shown in Figure 6(a) and Figure 6(b). Figure 6(d) shows the line voltage waveform THD of the five-level CHMLI which is 3.377%. The waveforms are balanced nearly sinusoidal with a fundamental frequency of 50 Hz.



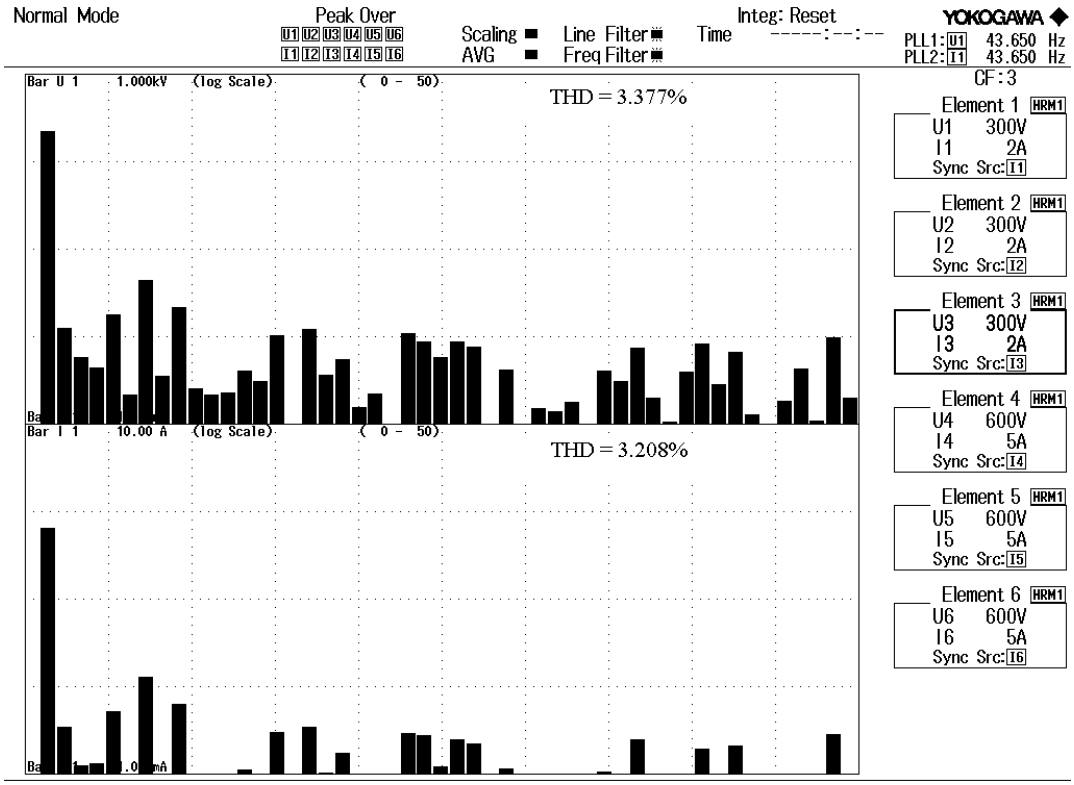
(a)



(b)



(c)



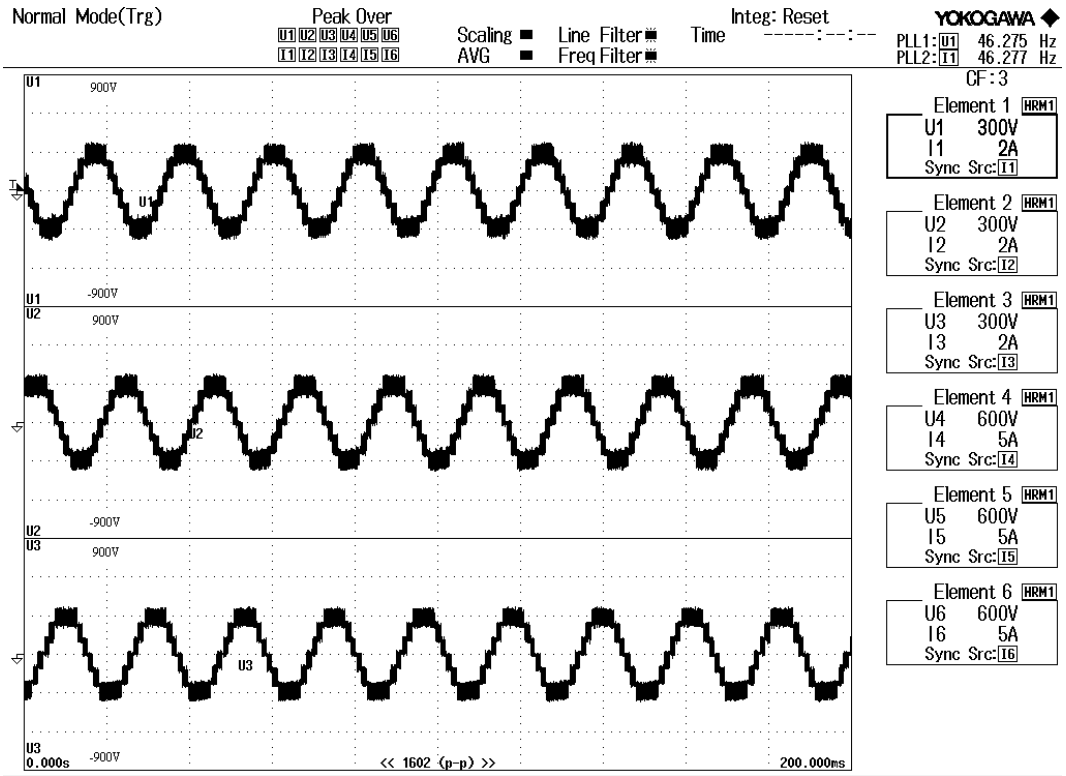
(d)

Figure 6. Experimental result of SVPWM for five-level CHMLI. (a) Phase voltage (Van); (b) Line-to-Line voltage (Vab); (c) Line current (Ia); (d) THD measurement for output voltage and output current.

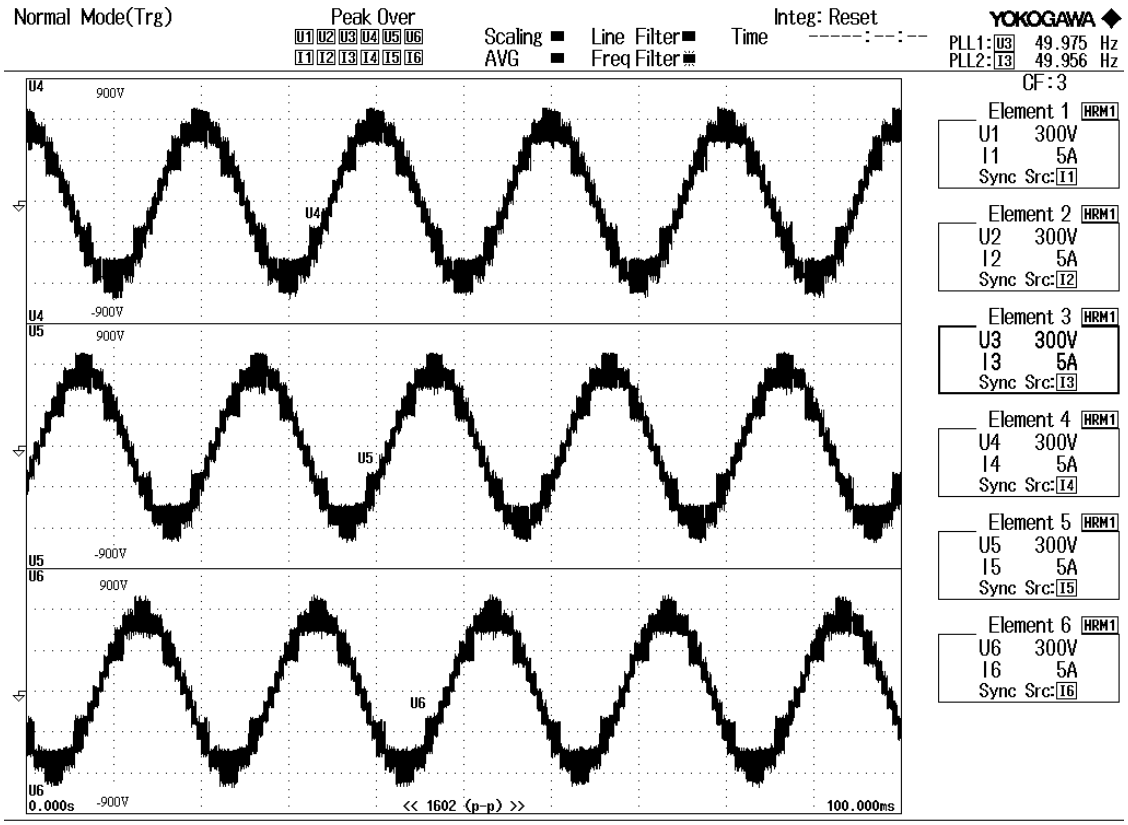
The phase voltage waveform, V_a, V_b and V_c are 120˚ displaced of each other as anticipated in the simulation. They exhibit some slight distortions in the waveforms which are shown by the tiny ripples and unsmooth sinusoidal waveforms. This is due to the existence of the small level of low order harmonics, e.g. 3th, 5th and 7th harmonics, centered around the cut-off frequency of the filter which can be clearly seen in the harmonic spectrum and comply with the requirement of IEEE-2000. The three-phase load current waveforms of five-level CHMLI are depicted in **Figure 6(c)**.

Like the voltage waveforms, current waveforms are balanced and as anticipated, the 50 Hz sinusoidal current waveforms are 120˚ displaced to each other. Owing to the existence of the 3th, 5th, and 7th harmonic components centered on the filter cut-off frequency, the current waveforms show slight distortions in the waveforms. As a result, the THD for the load current waveform of five-level CHMLI is calculated to be 3.208% as depicted in **Figure 6(d)** which complies with the requirement of IEEE-2000.

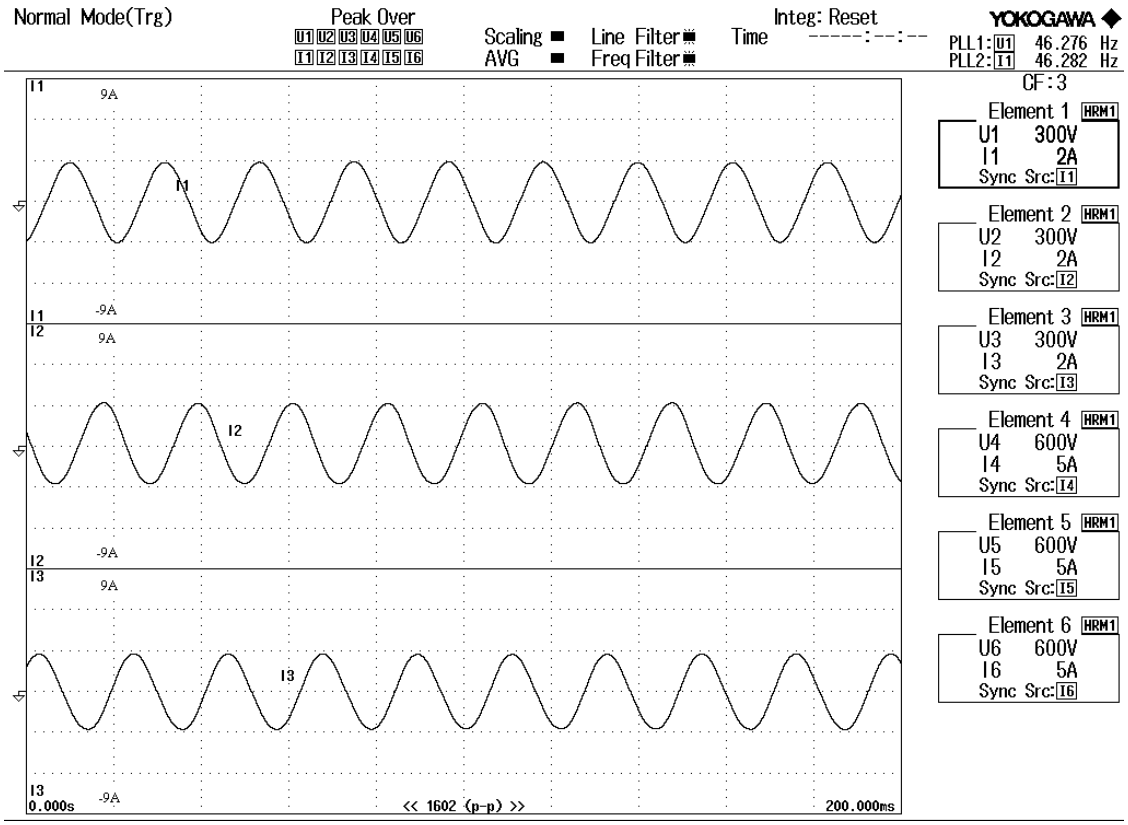
In view of the phase relation of load current and voltage waveform, both waveforms are in-phase or unity power factor condition, which implies an efficient of power transfer. The experimental result of the proposed PV three-phase seven-level CHMLI is shown in **Figures 7(a)-(d)**. All critical simulation and experimental parameters like PV array specifications, DC link capacitor sizes, H-bridge switching device specs, LC filter values, load parameters, and the tuned K_p and K_i gains of the PI controllers are based on [14]-[16].



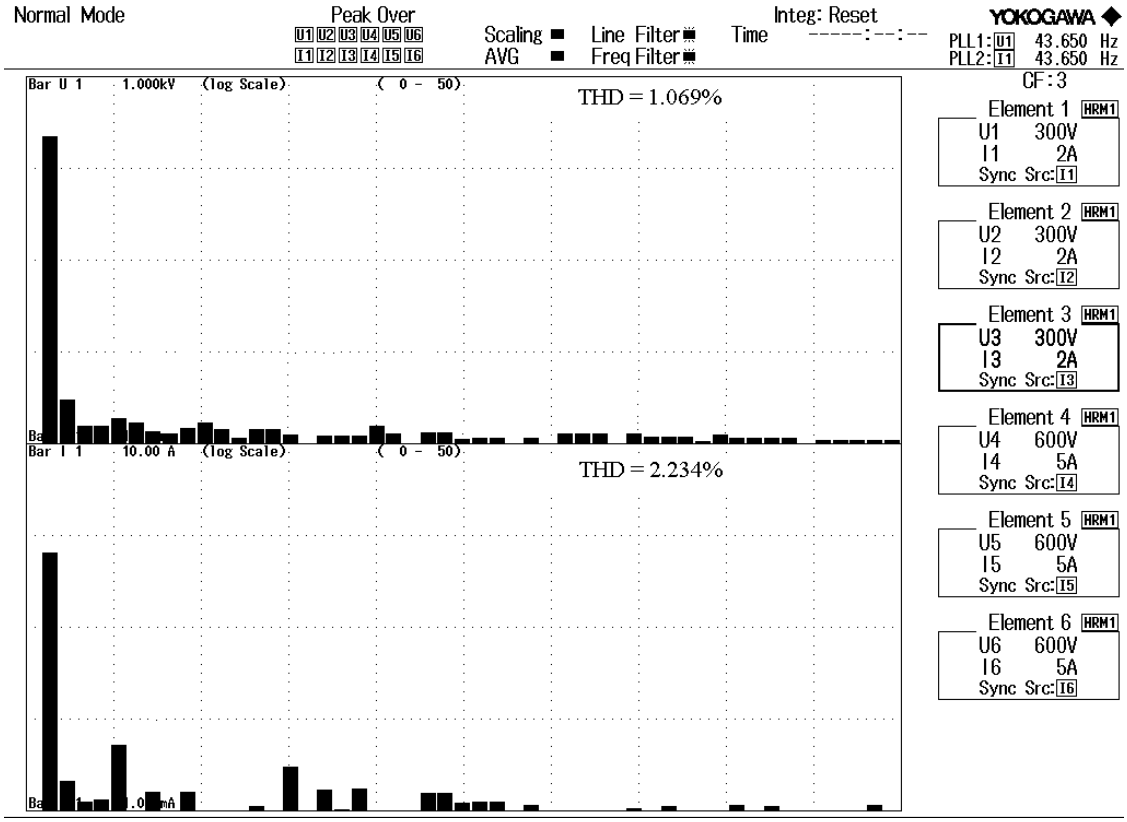
(a)


Normal Mode(Trg)
Peak Over
U1 U2 U3 U4 U5 U6
I1 I2 I3 I4 I5 I6
Scaling
AVG
Line Filter
Freq Filter
Integ: Reset
Time
YOKOGAWA
PLL1: U3 49.975 Hz
PLL2: I3 49.956 Hz
CF:3
U4 900V
U4 -900V
U5 900V
U5 -900V
U6 900V
U6 -900V
U6 0.000s
<< 1602 (p-p) >>
100.000ms
Element 1 HRM1
U1 300V
I1 5A
Sync Src: I1
Element 2 HRM1
U2 300V
I2 5A
Sync Src: I2
Element 3 HRM1
U3 300V
I3 5A
Sync Src: I3
Element 4 HRM1
U4 300V
I4 5A
Sync Src: I4
Element 5 HRM1
U5 300V
I5 5A
Sync Src: I5
Element 6 HRM1
U6 300V
I6 5A
Sync Src: I6

(b)


Normal Mode(Trg)
Peak Over
U1 U2 U3 U4 U5 U6
I1 I2 I3 I4 I5 I6
Scaling
AVG
Line Filter
Freq Filter
Integ: Reset
Time
YOKOGAWA
PLL1: U1 46.276 Hz
PLL2: I1 46.282 Hz
CF:3
I1 9A
I1 -9A
I2 9A
I2 -9A
I3 9A
I3 -9A
I3 0.000s
<< 1602 (p-p) >>
200.000ms
Element 1 HRM1
U1 300V
I1 2A
Sync Src: I1
Element 2 HRM1
U2 300V
I2 2A
Sync Src: I2
Element 3 HRM1
U3 300V
I3 2A
Sync Src: I3
Element 4 HRM1
U4 600V
I4 5A
Sync Src: I4
Element 5 HRM1
U5 600V
I5 5A
Sync Src: I5
Element 6 HRM1
U6 600V
I6 5A
Sync Src: I6

(c)



(d)

Figure 7. Experimental result of SVPWM for seven-level CHMLI. (a) Phase voltage (Van); (b) Line-to-Line voltage (Vab); (c) Line current (Ia); (d) THD measurement for output voltage and output current.

The output phase voltage and line voltage of the seven-level CHMLI is shown in **Figure 7(a)** and **Figure 7(b)**. **Figure 7(d)** shows the line voltage waveform THD of the seven-level CHMLI which is 1.069%. The waveforms are balanced nearly sinusoidal with a fundamental frequency of 50 Hz. The phase voltage waveform, V_a, V_b and V_c are 120˚ displaced of each other as anticipated in the simulation. They exhibit some slight distortions in the waveforms which are shown by the tiny ripples and unsmooth sinusoidal waveforms. This is due to the existence of the small level of low order harmonics, e.g. 3rd, 5th and 7th harmonics, centered around the cut-off frequency of the filter which can be clearly seen in the harmonic spectrum and comply with the requirement of IEEE-2000. Finally, the three-phase load current waveforms of seven-level CHMLI are depicted in **Figure 7(c)**. Like the voltage waveforms, current waveforms are balanced and as anticipated, the 50 Hz sinusoidal current waveforms are 120˚ displaced to each other. Owing to the existence of the 3rd, 5th, and 7th harmonic components centered on the filter cut-off frequency, the current waveforms show slight distortions in the waveforms. As a result, the THD for the load current waveform of seven-level CHMLI is calculated to be 2.234% as depicted in **Figure 7(d)** which complies with the requirement of IEEE-2000. In view of the phase relation of load current and voltage waveform, both waveforms are in-phase or unity power factor condition,

which implies an efficient of power transfer. In general, the above real hardware experimental results are slightly different compared to that of simulation. Unlike simulation, the experimental results might be influenced by the uncontrollable nature of parameters, e.g. component tolerance variation and circuit parasitic inductance and capacitance which affect the performance of the inverter especially the filter. Nevertheless, these results presented are considered a good conformity between the experimental and simulation.

7. Conclusion

This paper presents FPGA implementation of SVPWM control for a three-phase CHMLI for PV systems. The configuration for the proposed system is designed and simulated using MATLAB/Simulink and implemented on FPGA. This paper investigates the use of SVPWM can provide proper selecting switching states of the inverter and optimization of switching patterns. The fuzzy MPPT is integrated with the inverter so that a DC-DC converter is not needed and the output shows accurate and fast response. The simulation result gives output voltage and current waveforms are stabilized at 1 p.u. which proves that the algorithm employing PI controllers are effective for the output regulation. The proposed system guarantees a fast transient response, a high disturbance rejection capability, a robust performance and lower THD is obtained. The simulation results reveal that the generated voltage spectrum is improved in the SVPWM algorithm for seven-level CHMLI than five-level CHMLI. To validate the simulation results, a prototype of five-level and seven-level inverter has been developed and the proposed CHMLI model control algorithm managed to generate the ac output power from the PV modules. The captured experimental results show that the inverter controller produces stable sinusoidal output voltage and current of 50 Hz which is comparable to the simulation. The experimental results indicate that the voltage harmonics are highly reduced by the proposed SVPWM technique for seven-level CHMLI for PV system. The results obtained are full promise to use the CHMLI with SVPWM strategy are gained importance in PV generation system.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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