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Basic CMOS VLSI Circuits and Low Power Devices Employing Various Reduction Techniques to Reduce Leakage Power at Low Supply Voltage in Nanoscale Technology

Ghanshyam Singh

School of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India
Email: gshyamsingh2@gmail.com

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Abstract

In this work, the author proposed various techniques for reducing leakage power, leakage current, power consumption and power supply voltage. In this work, we implement CMOS Inverter, NAND Gate, CMOS VLSI Based AOI-OAI Circuits and Full Adder. We also compare all implemented circuits with LECTOR Technique and LECTOR Stack State techniques, which are inserted between pull-up and pull-down network Proposed technique simulation has been performed using HSPICE software in 32 nm, 45 nm, 90 nm, and 180 nm nanometer technology with a supply voltage range of 0.6 V - 1.0 V. The battery life of modern mobile computing, multimedia, wireless communication, and other real-time applications is increasing with LECTOR and LECTOR stack state reduction (LSSR). According to HSPICE simulated results by CMOS Inverter, NAND gate, CMOS VLSI Based AOI-OAI circuits and full adder circuits, subthreshold leakage current is decreased by 89% compared to the base case, 80% compared to LECTOR, and 34% compared to LECTOR Stack state reduction method and LECTOR transistor. We can achieve better leakage reduction by controlling supply voltage and by making the switching CMOS transistor.

Keywords

CMOS, Subthreshold Leakage Current, Leakage Control Transistor, LECTOR Stack State Reduction

1. Introduction

The rapid growth in semiconductor technologies through the use of deep submi-

cron processes has led to the function sizes of MOS gadgets shrinking, thereby integrating extraordinarily complicated functionality on a single chip. In the ever-growing advertising demands of cellular hand-held gadgets used all over the world nowadays, battery-powered digital systems are the backbone. To maximize the battery life and the amazing computational capacity or storage potential of multimedia-supportable gadgets and battery-operated notebook computer systems, personal communication devices consisting of cellular telephones, pocket computers, PDAs, hearing aids, and implantable pacemakers or defibrillators need to be found with very low power requirements. The development and fast growth in the semiconductor era have reduced the feature sizes by contracting or shrinking the MOS transistors via the usage of deep submicron approaches or nanoscale approaches. In sleep mode, to reduce leakage, the device is turned off. This approach affords a massive reduction in leakage with a minimum effect on performance. It's been shown that the energy gate technique makes use of high-voltage sleep transistors. With miniaturization and the growing trends and developments of the microelectronics era towards wireless communication, power dissipation and physical size have become very crucial design challenges. The power dissipation has not been completely removed, even with the scaling down of the supply voltage. The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area keeps increasing. The component failure rate approximately doubles for every 10˚C - 15˚C increase in the operating temperature of the portable devices. According to Moore's law, the manufacturing of on-chip devices doubles every 18 months or almost two years. Minimizing power consumption and physical size has become an extremely challenging area of research. These techniques also suffer from turning-on latency. The latency affects the control of leakage power. The Basic Structure of the static CMOS Leakage Source is reported in Figure 1.

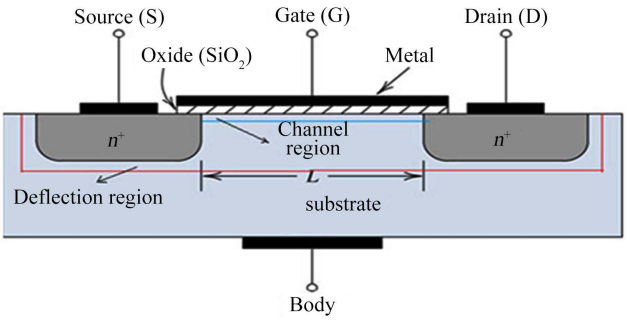

Figure 1. Basic structure of static CMOS leakage source.

2. Literature Survey

The literature reports a large number of techniques for reducing power dissipation and leakage current in CMOS and VLSI circuits. As CMOS technology continues to scale into deep-submicron and nanometer regimes, reducing the supply voltage has become essential for minimizing dynamic power consumption. However, technologies scaling also leads to a significant increase in leakage current, making

leakage power one of the major challenges in modern integrated circuit design. To overcome this issue, researchers have proposed numerous leakage reduction approaches, including advanced leakage reduction techniques, sub threshold leakage optimization in FinFET devices, leakage power modeling for deep-submicron technologies, and recent leakage suppression methods for power electronic converters such as three-level inverters [1]-[4]. Furthermore, power gating has emerged as an effective solution for ultra-low-power CMOS circuits, while transistor stacking, input vector control, and self-controllable voltage level techniques have been widely investigated to suppress standby leakage in digital circuits and SRAM cells [5]-[8]. Several studies have also focused on the analysis and characterization of leakage reduction methodologies, including body biasing, transistor stacking, and other device-level optimization techniques for deep-submicron CMOS technologies [9] [10]. In addition, novel low-power sequential circuits, such as pulse-triggered D flip-flops, energy-efficient SRAM cells, hybrid full adders, and dynamic body-biasing-based logic circuits, have been proposed to achieve significant reductions in both leakage power and overall energy consumption [11]-[15]. Various circuit-level optimization methods, including transistor stack techniques, multi-threshold CMOS (MTCMOS), pass-transistor-based pull-up/pull-down insertion, and low-power clocking schemes, have further demonstrated substantial improvements in power efficiency [16] [17]. Fundamental studies on modern VLSI devices have provided a comprehensive understanding of leakage current mechanisms and their impact on circuit performance [18]. Building upon these principles, several leakage control techniques, such as LECTOR (Leakage Control Transistor), Sleepy Keeper, Gated-VDD, SCCMOS (Super Cut-Off CMOS), and efficient transistor stack-based approaches, have been extensively explored for minimizing standby leakage without significantly affecting circuit performance [19]-[26]. Collectively, these studies demonstrate that a combination of device-level, circuit-level, and architectural optimization techniques is essential for achieving ultra-low-power and leakage-efficient CMOS circuit designs in advanced technology nodes.

2.1. Limitation of Various Reported Leakage Power Reduction Techniques in the Literature

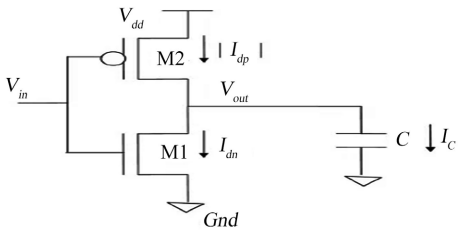

Figure 2. Shematic diagram of nanoscale basic base CMOS inverter with load capacitance.

2.2. Sleep Transistor Technique

In addition to the MTCMOS technique, high VT sleep transistor is introduced between V_{dd} (supply voltage) and pull up network, and between pull down net-

work and ground for high switching speed, where low VT transistors are used in the circuit. Efficient power management is done by a sleep control mechanism. This modified MTCMOS technique can only reduce the standby leakage power and the introduced MOSFETs result in an increase in area and delay. During standby mode, both sleep transistors get turned off, introducing large resistance in the conduction path and thus, leakage current is low. Isolation between V_{dd} and ground path is necessary for leakage reduction. This technique faces a problem for data retention purposes during sleep mode. The wake-up time and energy of the sleep technique have a significant impact on the efficiency of the circuit.

2.3. Multi Threshold CMOS and Dual V_T Technique

In Multi Threshold CMOS, two sleep transistors are presented between the supply voltage and ground. The sleep transistors are controlled by complementary sleep and sleep High-threshold NMOS gating transistor is connected between the pull-down network and the ground and low-threshold voltage transistors are used in the gate. Reverse conduction paths exist, which tend to reduce the noise margin. There also exists performance degradation due to the high-threshold transistors in series with all the switching current paths. MTCMOS technique adds higher values of V_{th} for sleep transistors between pull-up networks.

2.4. Dual V_T Technique

Dual V_T Technique is a variation in multi-threshold CMOS, in which the gates in the critical path employ low-threshold transistors and high-threshold transistors for the gates in the non-critical path. Both methods require additional mask layers for different values of V_T in the fabrication, which is a complicated task of depositing two different thin oxide layers. These are the earliest proposed techniques to reduce the leakage power. The Schematic Diagram of a nanoscale basic base CMOS Inverter with load Capacitance is shown in Figure 2.

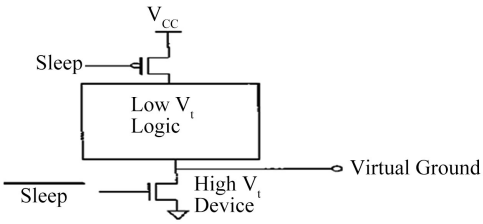

Figure 3. Schematic diagram of dual sleep VT and MTCMOS structure.

The schematic diagram of the dual sleep VT and MTCMOS structure is reported in Figure 3.

2.5. SLEEP Transistor or LECTOR Technique

The LECTOR or Sleep technique is developed to overcome the disadvantages of Dual VT and MTCMOS techniques. This is a state-destructive technique that cuts off either the pull-up or pull-down or both networks from the supply voltage or

ground or both using sleep transistors. Now we consider the resistance in the path; the propagation delay of the gate gets maximum. MOS transistors of LECTOR inverter are sized or scaled down such that the propagation delay is reduced or equal to its base case. In the sleep technique, the sleep transistors have to be able to isolate the power supply and ground from the rest of the transistors of the gate. Hence, they need to be made bulkier, dissipating more dynamic power. This offsets the savings yielded when the circuit is in idle condition. The sleep transistor technique depends on input vector conditions, and it needs additional circuitry to monitor and control the switching of sleep transistors, consuming power in both active and idle states. Two MOS transistors are added in LECTOR technique in every path from V_{dd} to ground irrespective of number of MOS transistors in pull-up and pull-down logic. Therefore, forced stacks have 100% area overhead. The loading requirement with LECTORs is a constant which is much lower. Whereas the loading requirements with forced stacks depend on the number of MOS transistors added. Hence, the performance degradation is insignificant in the case of LECTOR and we overcome the drawbacks faced by forced stack technique. V_{dd} is connected between pull-down networks and GND technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors.

2.6. Forced Stack Technique

In this technique, we can analyze the problems faced by the conventional CMOS circuits. Every transistor in the network is duplicated, with both the transistors bearing half the original transistor width. The duplicated transistors cause a slight reverse bias voltage between the gate and source when both transistors are turned off. The sub-threshold current is exponentially dependent on gate bias. It results in substantial current reduction.

2.7. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to V_{dd} and PMOS to GND. This creates virtual power and ground rails in the circuit, which affects the switching speed.

2.8. ZIGZAG Technology

ZIGZAG Technology is a novel approach named ZIGZAG KEEPER is proposed at the low-power circuit level for the reduction leakage current and area. It overcomes the limitations of sleep or vector techniques.

2.9. Leakage Feedback Technique

This technique is based on the sleep approach to maintain logic in sleep mode; Leakage feedback techniques use two additional transistors and are driven by the output of the circuit implemented, including leakage feedback. The performance degradation and increase in area are the limitations, along with the limitations of sleep technique.

3. Proposed CMOS VLSI Circuits

To achieve low power through LSSR is formed by combining LECTOR technique and LSSR. It has the features of both approaches and thus is more beneficial than the previous work done. The circuit is proposed by introducing two gated leakage transistors between pull-up and pull-down networks with high threshold voltage, and then stack effect is added to pull-up and pull-down networks by dividing each transistor into half-size transistors.

3.1. LECTOR Technique and LSSR Technique

The LECTOR Stack Reduction approaches, namely LECTOR and Force Track. Various circuit applications of the LECTOR technique and LSSR based are reported in this section. The LECTOR technique is applied to the following CMOS circuits, AOI and OAI and their respective base case is implemented to present the amount of leakage power reduced in LECTOR technique. LECTOR Based CMOS Inverter is reported in **Figure 4**.

3.2. Proposed Example 1 LECTOR CMOS Gate

The LECTOR CMOS gate presents two leakage control transistors introduced between the pull-up and pull-down network within the logic gate that is one PMOS for pull-up and one NMOS for pull-down, for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near-cutoff region. The proposed topology of a LECTOR CMOS gate yields the simulated DC characteristics of LECTOR Based NAND Gat is shown in **Figure 5**. The two LECTORs CMOS gates are introduced between nodes N1 and N2. The gate terminal of each LECTOR CMOS is controlled by the source of the other, hence termed as self-controlled stacked transistors. Leakage Control MOS Transistor, or LECTOR COMS technique, is illustrated in detail with the case of an inverter. The PMOS is reported as LECTOR 1 and a NMOS as LECTOR 2 between N1 and N2 nodes of inverter configuration. The output of inverter configuration is taken from the connected drain nodes LECTOR 1 and LECTOR 2. The source nodes of LECTOR 1 and LECTOR 2 are the nodes N1 and N2, respectively, of the pull-up and the pull-down network. The gates of LECTOR 1 and LECTOR 2 are controlled by the applied potential at the source terminal of LECTOR 1 and LECTOR 2, respectively. This type of connection always presents one of the two LECTORs in its near-cutoff region for all inputs. Dual Threshold Voltage Techniques for CMOS and Low Power VLSI Circuits are shown in **Figure 6** with the two LCTs added to pull-up and pull-down network between the V_{dd} and GND path. CMOS design style. Secondly, all the test circuits are implemented by NAND gates and analyzed using these variants. The stacking MTCMOS structure reduces the magnitude of leakage current and limits the energy consumption in transition mode resistance, allowing a conducting path. The resistance provided by LCT1, even though not equal to the OFF resistance, increases. The resistance in the path of supply voltage to ground

thereby reduces the sub-threshold leakage current, resulting in a reduction in leakage power. Similarly, when input A = 1, the voltage at the node N1 is 180 mV; hence LCT2 will be operated in near cutoff state. The states of all transistors in the LECTOR inverter for all possible inputs are tabulated in Table 1. When V_{dd} = 1 V, input A = 0, the voltage at node N2 is 760 mV. LCT1 cannot be LECTOR Based CMOS Inverter and is presented in Figure 4.

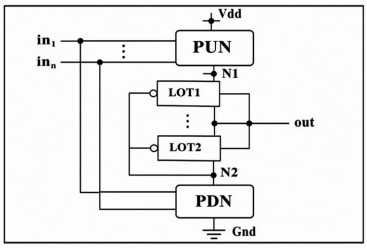

Figure 4. LECTOR Based CMOS Inverter.

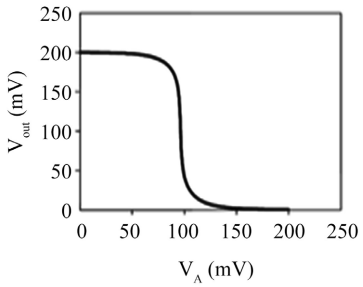

Figure 5. Simulated DC characteristic of LECTOR based NAND gate.

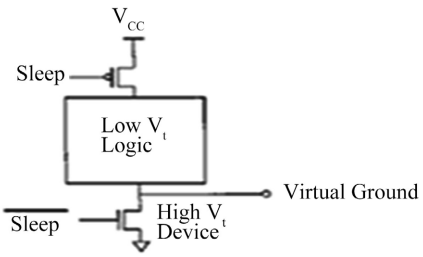

Figure 6. Dual threshold voltage techniques.

For CMOS and Low Power VLSI Circuits

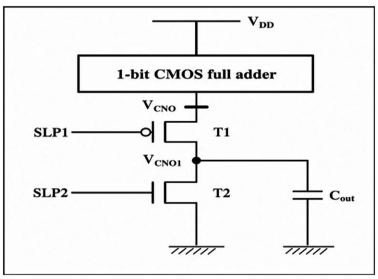

Figure 7. 1 Bit CMOS full adder employing MTCMOS stacking approach to reduce leakage current.

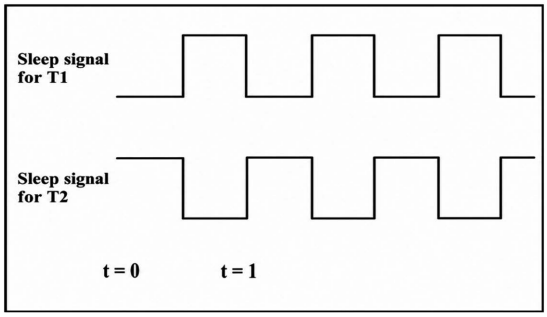

Figure 8. Simulated output of proposed LECTOR based CMOS inverter.

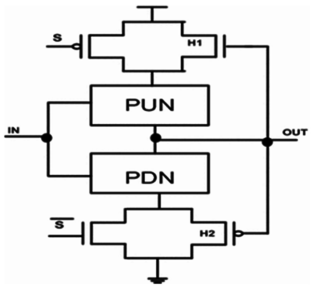

Figure 9. Proposed AOI and OAI CMOS circuit.

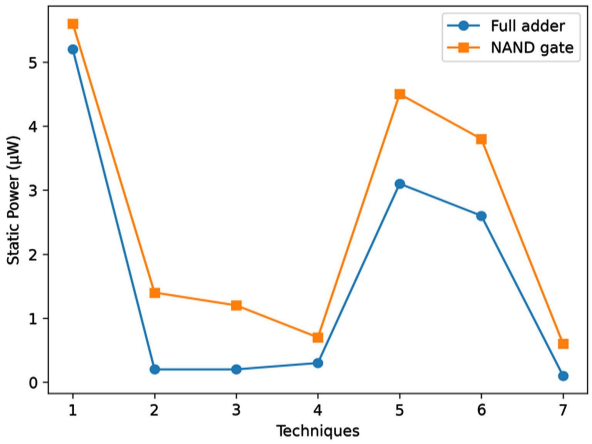

Figure 10. Static threshold sleep transistor technique for low leakage and high speed in CMOS VLSI circuits and low power device.

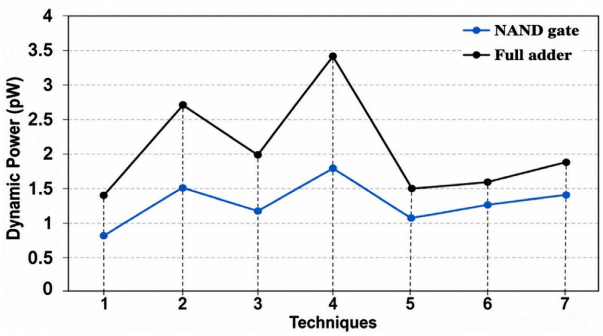

Figure 11. Dynamic threshold sleep transistor technique for low leakage and high speed in CMOS VLSI circuits and low power devices.

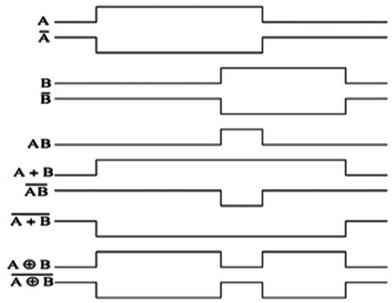

Figure 12. Transient waveform of AOI and OAI CMOS circuit.

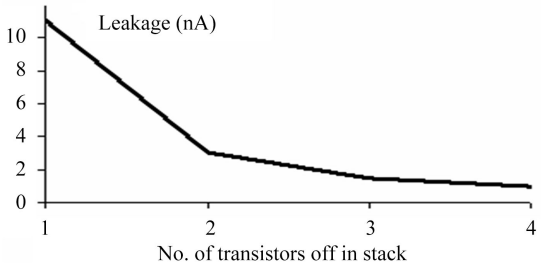

Figure 13. Transistor-stacking vs leakage current.

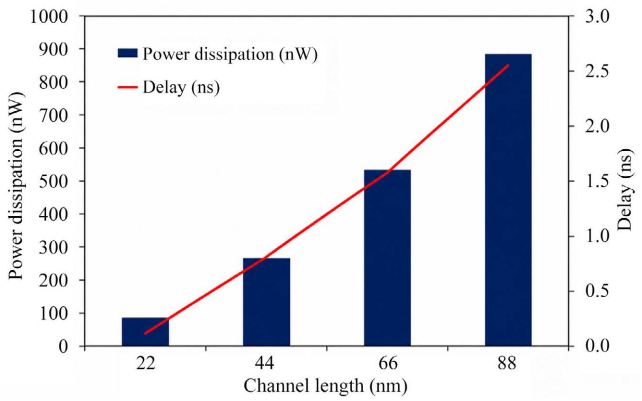

Figure 14. Presents power dissipation (nW) vs delay (ns), delay depends on channel length.

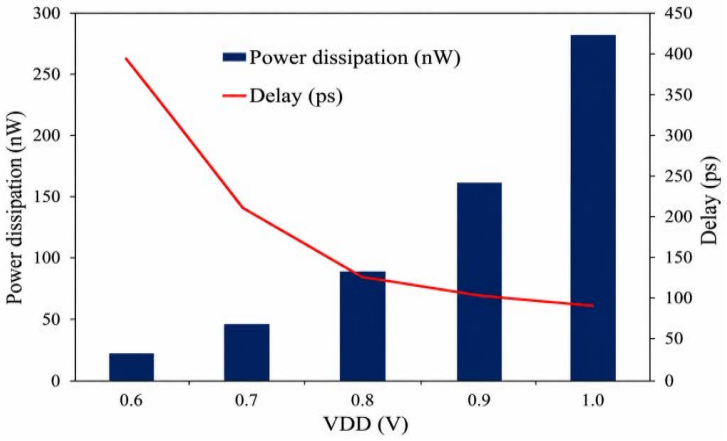

Figure 15. Simulated Result shows a plot of the corresponding values of power dissipation (nW) vs delay (ps).

Table 1. Simulated power dissipation and propagation delay of different circuits for CMOS process 180 nm technology.

Circuit Types	Power Dissipation (μW) at Various Input Vectors				Average Power (μW)	Delay (ns)	Switching Response
	P (0, 0) μW	P (0, 1) μW	P (1, 0) μW	P (1, 1) μW			
LECTOR Full Adder	0.96	0.08	1.0	0	0.51	3.19	Moderate
Stack Full Adder	0.61	0.25	0.43	0	0.32	2.27	Fast
LECTOR CMOS Inverter	1.05	0.17	0	0	0.305	3.39	Moderate
Stack CMOS Inverter	0.85	0.11	0	0	0.24	2.09	Fast
LECTOR CMOS NAND Gate	2.42	0.015	2.47	0.84	1.44	7.78	Slow
Stack CMOS NAND Gate	1.51	0.23	2.01	0.36	1.03	6.09	Slow

Table 2. Simulated power dissipation and propagation delay of different circuits for CMOS Process 90 nm technology.

Circuit Types	Power Dissipation (μW) at Various Input Vectors				Average Power (μW)	Delay (ns)	Switching Response
	P (0, 0) μW	P (0, 1) μW	P (1, 0) μW	P (1, 1) μW			
LECTOR Full Adder	0.73	0.06	0.75	0	0.38	2.45	Moderate
Stack Full Adder	0.45	0.18	0.31	0	0.23	1.78	Fast
LECTOR CMOS Inverter	0.77	0.14	0	0	0.227	2.75	Moderate
Stack CMOS Inverter	0.65	0.08	0	0	0.182	1.66	Fast
LECTOR CMOS NAND Gate	1.80	0.10	1.83	0.64	1.09	6.19	Slow
Stack CMOS NAND Gate	1.42	0.18	1.51	0.26	0.842	4.89	Moderate

The simulated power dissipation and propagation delay of different circuits are tabulated in **Table 1**. The simulated static power, total power and delay of NAND,

CMOS inverter, FULL ADDER and their LECTOR and stack gates are shown in Table 2. Dynamic power, total power and delay of NAND, CMOS inverter, FULL ADDER and their LECTOR and Stack gates are presented in Table 3. A 1 Bit CMOS full adder employing MTCMOS stacking is shown in Figure 7. The simulated output of the proposed LECTOR based CMOS inverter is shown in Figure 8. Figure 9 shows the proposed AOI and OAI CMOS circuit and the static and dynamic results. Threshold sleep transistor technique for low leakage and high speed in CMOS VLSI circuits and low-power devices is reported in Figure 10 and Figure 11. The simulated Transient Waveform of AOI and OAI CMOS circuit is presented in Figure 12. Transistor-stacking vs leakage current is shown in Figure 13. Figure 14 shows that the power dissipation and delay values increase with channel length. The simulated graph shows that channel length increases and V_{dd} (V). The simulated result shows a plot of the corresponding values of power dissipation (nW) vs delay (ps) in Figure 15. The channel length variation effect on power dissipation and delay metrics using the MTCMOS approach is reported in Figure 16.

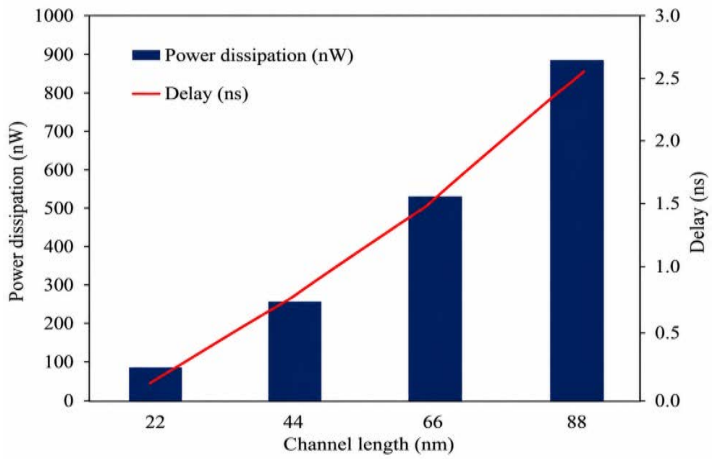

Figure 16. Represents channel length variation effect on power dissipation and delay metrics using the MTCMOS approach.

4. Experimental and Simulation Results

CMOS simulation processes have been performed using HSPICE software in 32 nm, 45 nm, 90 nm, and 180 nm with model of Berkeley Predictive Technology Model parameters for the standard CMOS at room temperature with supply voltage 0.6 V - 1.0 V to estimate delay, static and dynamic power, and power consumption. Table 1 presents the simulated power dissipation and propagation delay of different circuits, and Table 2 yields the static and total power delay of NAND GATE, CMOS Inverter, FULL ADDER, LECTOR, and Stack Gates. In order to compare the proposed technique with the base case and other techniques: LECTOR and LECTOR Stack State Reduction for CMOS Inverter, AOI-OAI Circuits, NAND gate and 1-bit full adder circuits have been implemented. Simulation results for CMOS Inverter, AOI-OAI Circuits, NAND gate and 1-bit full adder circuit cases have been measured with random input vector values changing every

clock cycle. According to simulation results represented in graphs and regarding the number of transistors used, a significant decrease in sub-threshold current, approximately 2 to 4 times in both NAND and Full Adder circuits, has been achieved, compared to traditional and other designs. There is an acceptable propagation delay compared to the base case concerning the high-resistance path LECTOR network and also a slight difference in dynamic power. Inputs of Full Adder have been adjusted so that they can change status in different input vector values or logic levels (0, 0), (0, 1). (1, 0), (1, 1). The outputs of circuits (sum, carry) without pass transistors have been shown according to inputs as Ain, Bin, and Cin, yielding the effect of using switching transistors, which has caused a considerable decrease in propagation delay. Through the simulation waveforms and the characteristics of LECTOR AOI resemble the base case. The LECTOR implementation involves the addition of two LCTs in each gate between the supply and ground path. For a particular MOS transistor, whenever the applied gate-to-source voltage is less than the threshold voltage of the transistor, there is no flow of current. Mathematically, when $I_{ds} = 0$ at $V_{gs} < V_t$. Tunneling through the gate oxide occurs because the thickness of the gate oxide layer is gradually reduced as technology is reduced to nanometers. The gate oxide tunneling current is caused by tunneling of electrons through an nMOS capacitor with a heavily doped n + polysilicon gate and a p-type substrate. Simulation for the 2-input NAND is performed by taking four different process parameters, viz. 32 nm, 45 nm, 65 nm. 90 nm and 180 nm. From the simulation, we analyze that as we scale down the technologies in the deep submicron regime, leakage current dominates. It is observed that when we move from 180 nm towards 45 nm, leakage current increases drastically up to 94.94% due to the reduction of the threshold voltage of CMOS transistor; as we scale down the channel length, leakage current increases. We observe that maximum leakage current flows at (1, 1) input vector combinations at 32 nm, 45 nm, 90 nm and 180 nm CMOS technology, respectively. All the simulations are performed using BPTM libraries in HSPICE simulator at 32 nm, 45 nm, 90 nm and 180 nm, with a load capacitance of 1 pF at 10 MHz frequency at supply voltages of 1.8 V, 1.5 V, 1.2 V, 1 V and 0.9 V. Metal-oxide-semiconductor field-effect transistor (MOSFET) channel length variation effect employing input-controlled stacking (MTCMOS) approach. The MOSFET's channel length affects the overall performance of the logic circuits. The channel length varies from 22 nm to 88 nm to obtain the channel length variation. Further, the channel lengths of NMOS and PMOS devices are considered equal. The widths of the NMOS and PMOS devices are maintained at 2 and 4 times the channel length, respectively. The supply voltage is a key factor that affects power dissipation and propagation delay. The effect of supply voltage variation on the proposed MTCMOS and LSSR approaches is investigated by varying the supply voltage from 0.6 to 1.0 V. The effect of supply voltage variation on input-controlled stacking (LECTOR and LSSR approaches) is investigated. There are 4 possible combinations for 2-input NAND; hence, the average of the four power dissipations gives the leakage power. In the case of 4-input AOI, power dissipations corresponding to all the 16 combinations are averaged. For a full adder, the average of 8 power dissipations is

the static power dissipated. LECTOR uses two LCTs, which are self-controlled transistors. LECTOR and LSSR present efficient reduction in leakage power, like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc., along with the advantage of not affecting the dynamic power. Since this technique does not require any additional control and monitoring circuitry and also in this technique, the exact logic state is in each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with the same set of input vectors. Static or leakage power dissipation is leakage currents, reverse-biased currents and substrate injection currents, which flow through the transistors in their steady states. Threshold voltages, to achieve high performance and low dynamic power dissipation, become more significant with the deep-submicron and nanometer technologies and thus it becomes a great challenge to overcome the problem of leakage power. International Technology Roadmap for Semiconductors indicates that leakage power consumption dominates the total chip power consumption as technology advances to the nanoscale. In future mobile computing, multimedia-supporting devices and mobile communication applications are fully restricted by their large supply voltage and battery life; battery life is a major concern. The proposed techniques can be implemented in CMOS Circuits as well as low-power VLSI circuits and save the power consumption of the chip, which leads to increased battery life. The simulated power dissipation and propagation delay of various circuits for CMOS Process 45 nm Technology are reported in Table 3 and the simulated power dissipation and propagation delay of various circuits for CMOS Process 45 nm Technology are reported in Table 4. Dynamic power, total power and delay of NAND, CMOS inverter, FULL ADDER and their LECTOR and Stack gates are reported in Table 5.

Table 3. Simulated power dissipation and propagation delay of different circuits for CMOS process 45 nm technology.

Circuit Types	Power Dissipation (μW) at Various Input Vectors				Average Power (μW)	Delay (ns)	Switching Response
	P (0, 0) μW	P (0, 1) μW	P (1, 0) μW	P (1, 1) μW			
LECTOR Full Adder	0.53	0.06	0.55	0	0.285	2.05	Moderate
Stack Full Adder	0.34	0.13	0.23	0	0.175	1.52	Fast
LECTOR CMOS Inverter	0.59	0.11	0	0	0.175	2.31	Moderate
Stack CMOS Inverter	0.45	0.06	0	0	0.13	1.36	Fast
LECTOR CMOS NAND Gate	1.32	0.09	1.35	0.46	0.80	5.59	Slow
Stack CMOS NAND Gate	1.02	0.12	1.11	0.22	0.617	4.19	Moderate

Table 4. Simulated power dissipation and propagation delay of different circuits for CMOS process 32 nm technology.

Circuit Types	Power Dissipation (μW) at Various Input Vectors				Average Power (μW)	Delay (ns)
	P (0, 0) μW	P (0, 1) μW	P (1, 0) μW	P (1, 1) μW		
LECTOR Full Adder	0.48	0.04	0.49	0.51	0.380	0.016
Stack Full Adder	0.78	0.07	0.78	0.83	0.610	0.024
LECTOR CMOS Inverter	0.26	0.017	0.28	0.29	0.211	0.009
Stack CMOS Inverter	0.38	0.030	0.39	0.40	0.30	0.010
LECTOR CMOS NAND Gate	0.38	0.028	0.40	0.42	0.307	0.013
Stack CMOS NAND Gate	0.48	0.035	0.50	0.51	0.381	0.016

Table 5. Dynamic power, total power and delay of NAND, CMOS inverter FULL ADDER and their LECTOR and stack gates.

Circuit Type	Dynamic Power (μW) at Various Input Vectors				Delay (ns)
	0, 0	0, 1	1, 0	1, 1	
LECTOR STACK FULL ADDER	0.391	0.033	0.399	0 nw	1.871
STACK FULL ADDER	0.248	0.101	0.173	0 nw	1.333
LECTOR CMOS Inverter	0.418	0.074	0 nw	0 nw	1.946
STACK CMOS Inverter	0.342	0.044	0 nw	0 nw	1.195
LECTOR NAND	0.971	0.059	0.991	0.342	5.015
STACK NAND	0.769	0.097	0.810	0.148	3.878

Table 6. W/L ratio for NMOS.

S.No	Technology Used	W (μm)	L (μm)	W/L
1.	180 nm	0.36	0.18	2.0
2.	90 nm	0.18	0.09	2.0
3.	45 nm	0.09	0.045	2.0
4.	32 nm	0.064	0.032	2.0

W/L ratios for NMOS and PMOS transistors are reported in Table 6 and Table 7. Total power, dynamic power and leakage power vs operating voltage is reported in Figure 17 and normalized delay vs V_{dd} is shown in Figure 18.

Table 7. W/L ratio for PMOS.

S.No	Technology Used	W (μm)	L (μm)	W/L
1.	180 nm	0.72	0.18	4.0
2.	90 nm	0.36	0.09	4.0
3.	45 nm	0.18	0.045	4.0
4.	32 nm	0.128	0.032	4.0

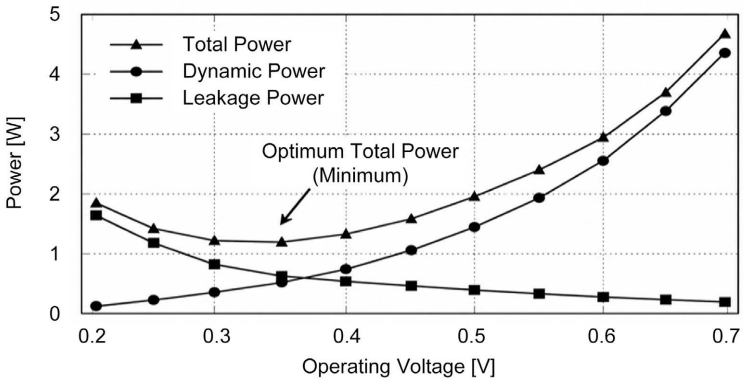

Figure 17. Presents total power, dynamic power and leakage power vs operating voltage.

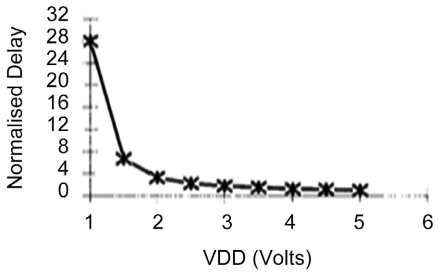

Figure 18. Normalized delay vs V_{dd}.

5. Conclusions and Suggestions

In this paper, the LSSR technique is presented as a more efficient method for NAND, CMOS circuits, and full adder circuits in 32 nm technology with a 0.6 V power supply. Based on the results, LSP, compared to other approaches such as MTCMOS, LECTOR and Forced STACK, had better operation in reducing leakage power. Therefore, sub-threshold current has been reduced by 89% in relation to the base case, 76% compared to LECTOR, and 23% compared to Sleepy Keeper. Also, propagation delay has been improved, so that this technique is suitable for high-speed circuits in DSM regime. In the future, the LSP technique as one of the combined designs will be implemented in the field of VLSI systems to improve consumption power and sizing of integrated circuits. Increasing leakage power

due to scaling down of device dimensions, supply and Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. The proposed techniques yield some advantageous features, which are presented as:

1) When logic 0 is applied at the input terminal of CMOS, the NMOS transistor will turn OFF and PMOS will turn ON. As a result, logic 1 will be available at the output node.

2) When logic 1 is applied at the input, NMOS turns ON and PMOS goes into the OFF state. Thus, there will be logic 0 at the output node. Power dissipation in CMOS transistors occurs mainly because of the device switching operations.

3) The dynamic and short-circuit power dissipation are jointly called switching power dissipation. Switching power dissipation arises due to the charging and discharging of output load capacitance during switching.

4) During charging and discharging operation, there is an inevitable energy loss of CV^2 for static CMOS circuits. During charging operation, the energy dissipation through the pull-up block from the power supply is equal to CV^2, of which half of the energy ($0.5\ CV^2$) is stored.

5) There are 4 possible combinations for a 2-input NAND; hence, the average of the four power dissipations gives the leakage power.

6) In the case of 4-input AOI, power dissipations corresponding to all the 16 combinations are averaged.

7) For a multiplexer, the average of 64 power dissipations is considered and for a full adder, the average of 8 power dissipations is considered to be the static power dissipated.

8) LECTOR uses two LCTs, which are self-controlled transistors.

9) LECTOR and LSSR present efficient reduction in leakage power like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc., along with the advantage of not affecting the dynamic power.

10) Since this technique does not require any additional control and monitoring circuitry and also in this technique, the exact logic state is in each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with the same set of input vectors.

11) Static or leakage power dissipation is leakage currents, reverse-biased currents and substrate injection currents, which flow through the transistors in their steady states.

12) This work presents a comparative analysis of CMOS Process Technology 180 nm to 32 nm and the simulation results of various circuits in CMOS Process Technology 180 nm to 32 nm shows a significant performance, overall concluding remark 32 nm yields high performance due to less power dissipation and lower propagation delay. Therefore, CMOS Process 32 nm Technology is highly suitable for high-speed and low-power VLSI applications with Lecter Technique.

Suggestions

1) Manuscript yields a new circuit technology and comparative study.

2) Simulation results show that the proposed approach improves leakage current characteristics and enhances battery life in various mobile computing, multimedia, wireless communication and low-power real applications.

Conflicts of Interest

The author declares no conflicts of interest regarding the publication of this paper.

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